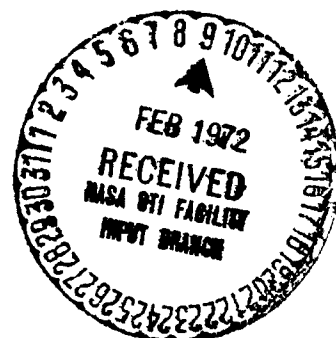# DIRECT MODELING, PARAMETER SIGNATURE ANALYSIS, AND FAILURE MODE PREDICTION OF PHYSICAL SYSTEMS USING HYBRID COMPUTER OPTIMIZATION

FINAL REPORT

$CR-123535$

Report No. RLD-3-71
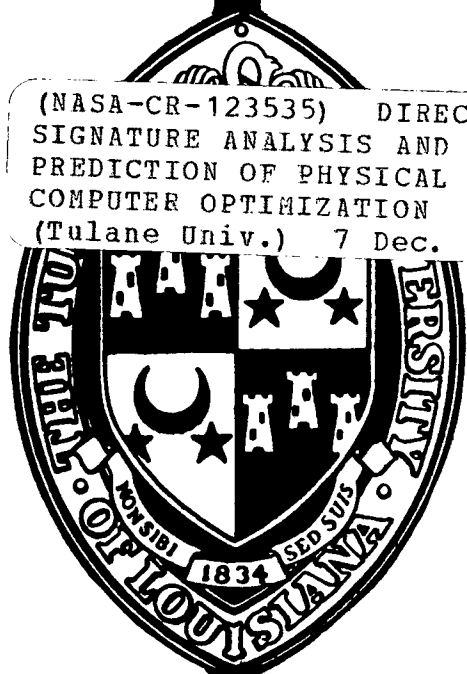
Robert L. Drake

Paul F. Duvoisin

Abhaya Asthana

Thomas W. Mather

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PART I INTRODUCTION

The work described in this report is concerned with high-speed automated identification and system design of dynamic systems, both linear and nonlinear. Special emphasis has been placed on developing hardware and techniques which are applicable to practical problems so practical feasibility generally has been examined as described in the report.

As indicated in the table of contents the basic modeling experiment and new results are described in Part 2. Using the improvements developed under this contract, successful identification of several systems, including a physical example as well as simulated systems, has been obtained. Using these methods the advantages of parameter signature analysis over signal signature analysis in "go-no go" testing of operational systems have been demonstrated. The feasibility of using these ideas in failure mode prediction in operating systems has also been investigated.

An improved digital controlled nonlinear function generator has been developed, de-bugged, and completely documented. Examples of the application of this device to practical problems is also described in Part 3.

The work reported here has suggested several extensions and new ideas some of which are currently in progress as reported in Part 4. In addition, this work has had an effect upon the academic program as outlined in Part 5. The conclusions reached from this work follow in Part 6. The report is completed by the references given in Part 7 and the program details and personnel descriptions given in the appendices of Part 8.

PART 2 DESCRIPTION OF EXPERIMENTS AND RESULTS

A. Basic Modeling Experiment

The basic modeling technique in use has previously been reported
[1, 2, 3] and is described in Figure 2-1. The technique consists of insert-
ing the proposed model in parallel with the actual system (in real time iden-
tification experiments) or in parallel with a function generator which pro-
vides an output identical to that of the actual system (in off-line identi-
fication) or identical to the desired output (in off-line system synthesis
problems).

An error signal is generated from the difference of the actual (or de-
sired) output signal and the model output signal. A positive definite
function of the error signal provides an index of performance (P). This in-
dex of performance is digitized and used as the input to the optimization
program in residence in the digital computer portion of the system. The
output of the optimization program is a new set of parameters which is in-
serted in the model equations. The optimization program adjusts the model
parameters until a minimum of the performance index is obtained. The out-
put printer then provides the best parameters of the model and the best
performance index obtained. The response of the best model and the actual
(or desired) response are available on an oscilloscope for high-speed systems
or on a plotter for low-speed systems.

In this work hybrid computation has been used primarily. As previously
reported and again verified in this work, the speed advantage of hybrid com-
putation compared with all-digital computation is of the order of 100/1.
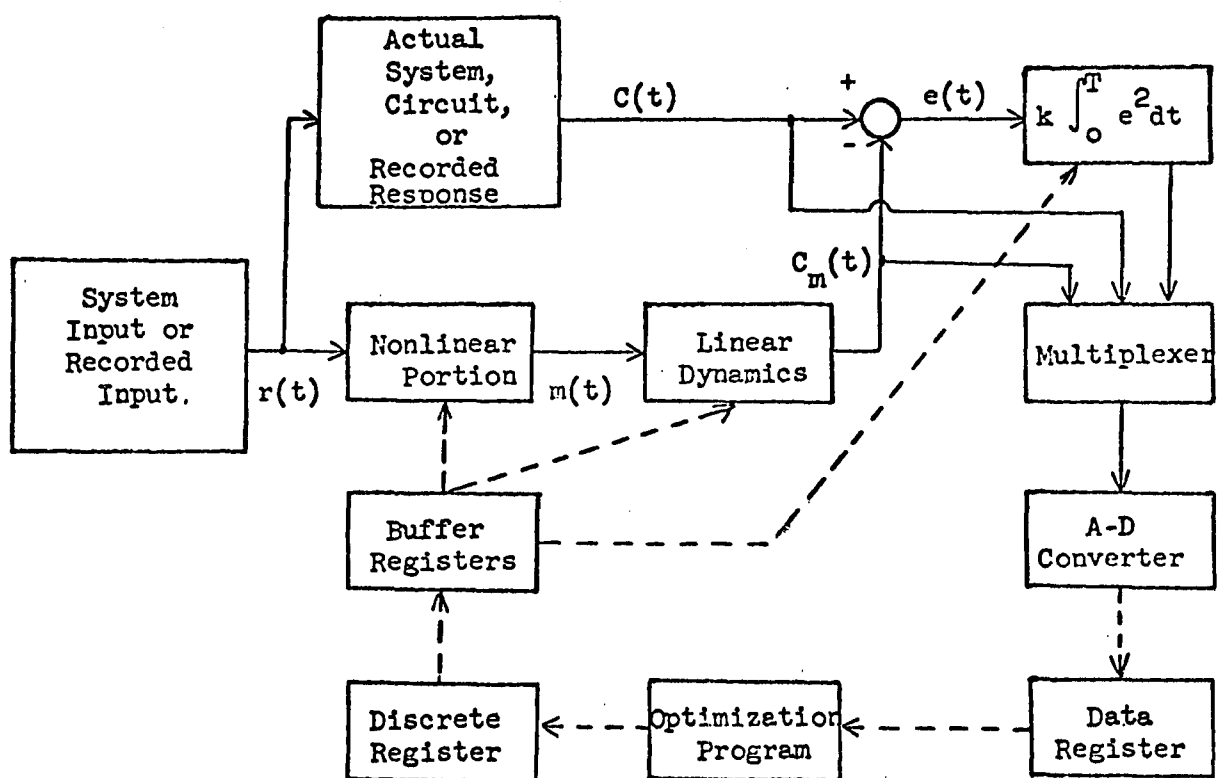
Figure 2-1   Basic Modeling Method

The equipment cost ratio is still approximately 10/1 favoring hybrid computation and the operational cost ratio is still about 5/1 favoring hybrid computation. Furthermore, as shown in Part 2(B) (3) below there are many physical electromechanical systems that are fast enough that high speed integration by analog components must be used in order to provide identification in near real time.

B.   New Results Under This Contract

The previous modeling work has been improved in several ways and extended in several directions during the work performed under this contract. A discussion of these improvements and extensions, with typical results, follow.

1).   Improvements In the Optimization Program

The optimization program in use in previous work implemented one-parameter (relaxation) search or normal steepest descent search. In this work the optimization program has been improved to include the Fletcher-Reeves algorithm [4,5]. A flow chart of the method now in use and a machine language listing (Athena computer) is included in the appendices. The inclusion of the Fletcher-Reeves search algorithm in the hybrid mode resulted in a less volatile search near the optimum, as reported in all-digital operations.

In addition, the facility for including general nonlinearities in the system model has been added. This has resulted from the design and construction of a digital controlled nonlinear function generator (DCNFG) and modification of the optimization program to control this device. The detailed design and implementation of this device is included in Part 3 (B) below and its use in solving certain

problems related to this work is mentioned in Part 3 (C) (1), (2) below.

2). Typical Simulation Results

Several simulation problems with widely different time scales have been solved using the improved optimization technique. The use of simulation allowed problems with known solutions to be set up in the laboratory. This was important to allow de-bugging of the program and to provide confidence in the modified technique, as well as to provide indications of the accuracy in parameter estimates that result.

Typical results at high speed are shown in Figure 2-2. The simulated system was linear third-order underdamped system with no zeros; therefore, there were 4 parameters to be obtained, including the system gain constant. The output of the simulated system following a step input is shown at the top of the figure. This transient required about 25 milliseconds and the total running time following the steps in about 50 milliseconds per pass. The middle figure shows several transients that resulted at the output of the model as the optimization program modified the model parameters. The lower figure shows the performance index (IAE) that resulted from several passes and indicates the improvement obtained during the optimization process. The process typically requires 10-20 passes to converge within, typically, 3 per cent of all parameters starting with, typically, 25-100 per cent error in the elements of the parameter vector. The total time involved for the process shown is typically 3-5 seconds including reset time for the analog components.
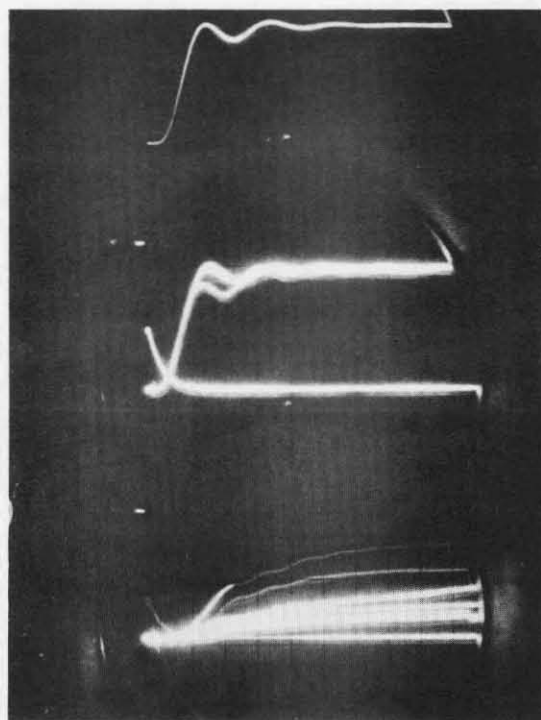
Figure 2-2 Simulation Results-High Speed

Using faster reset circuits for the analog components could reduce this by a factor of 2/3. A significant fraction of this time is attributable to the slow output device, since the total processing time is only on the order of one second. Measurable improvement in the accuracy of the parameter estimates and speed of convergence. is obtained by using the Fletcher-Reeves algorithm mentioned above, as compared with steepest descent.

Figure 2-3 (a) shows similar results with a much slower simulated system. The total time of the transients shown was about 15 seconds. The upper graph shows the convergence of the model response to the (simulated) actual response. The middle graph shows the improvement in the index of performance as the program modifies the model parameters and the lower figure shows the graph of the modeling error as the model is improved. Figure 2-3 (b) provides a summary of the results of this particular experiment.

Other problems have been solved with similar results at speeds between the speeds of the examples above.

3). Physical Example

In order to test the feasibility of the identification method under the rigors of practicality, a physical experiment (as opposed to a simulation) was set up in the laboratory. The experiment consisted of simply replacing the simulated system in the simulation experiments with a position servomechanism. The input and output of the position servomechanism were connected into the system as shown in Figure 2-1. No special precautions against noise were taken. The connections were
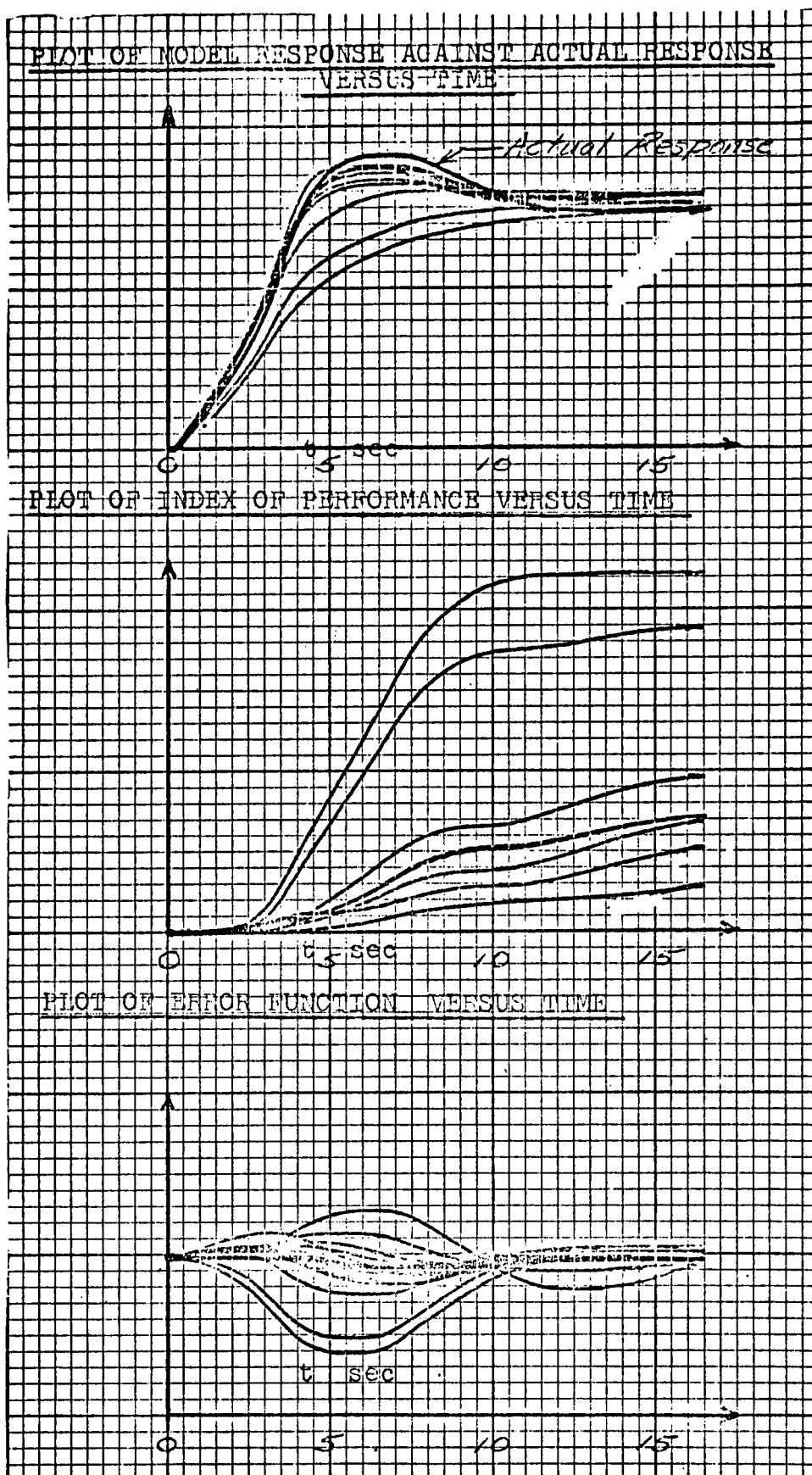
Figure 2-3(a) Typical Simulation Results-Slow Speed

RESULTS :

PARAMETER SETTINGS ON THE ACTUAL SYSTEM(SEE ANALOG COMPUTER DIAG.

PARAMETER 1	-	0.300
PARAMETER 2	-	0.125
PARAMETER 3	-	0.200

PARAMETER SETTINGS ON THE MODEL SYSTEM

INITIAL PARAMETERS		PARAMETERS AFTER CONVERGENCE
PARAMETER 1	0.600	0.3086
PARAMETER 2	0.320	0.1157
PARAMETER 3	0.200	0.2003

OCTAL PRINT OUT FROM ATHENA DIGITAL COMPUTER AFTER CONVERGENCE

00000745	BEST VALUE OF ALPHA FOR RUN 1
00000202	BEST VALUE OF ALPHA FOR RUN 2
00000202	BEST VALUE OF ALPHA FOR RUN 3
00000270	BEST VALUE OF ALPHA FOR RUN 4
00002324	BEST VALUE FOR PARAMETER 1
00000737	BEST VALUE FOR PARAMETER 2
00001461	BEST VALUE FOR PARAMETER 3
00000340	MINIMUM VALUE FOR PERFORMANCE INDEX

```
C  O  O  O  O  7  4  5
C  O  O  O  O  2  O  2
O  O  O  O  O  2  O  2
O  O  O  O  O  2  7  O
O  O  O  O  2  3  2  4
O  O  O  O  O  7  5  7
O  O  O  O  1  4  6  1
7  7  7  7  3  1  O  7
O  O  O  O  O  3  4  O
```

Figure 2-3(b) Typical Simulation Results-Slow Speed

made with open wire leads of about 8 feet length.

The results are indicated in Figure 2-4. The figure shows the
convergence of the model response to the actual servomechanism response
for 3 different starting guesses of the model parameters. In each
case the servomechanism response to a step input is at the top, the
model responses to the same step is in the center, and the performance
index on successive passes is at the bottom. The total transient
shown takes about 150 milliseconds and is followed by a reset inter-
val of approximately the same length. The identification process
required, typically, about 100 integrations of the model equations
or 15-30 seconds total time depending upon the reset time alloted.
It is interesting to note at this point that digital integration of
the model equations requires about 15 seconds per integration, or
about 25 minutes for an identification of a low order system and
considerably longer for a higher order system. Included in Figure
2-4 is an octal printout of the performance index, the four parameters
being optimized in the model, and the value of α in the optimization
program after the optimization of the model is completed.

4). Parameter Signature Analysis - Concept and Typical Test Results

A new concept suggested and investigated in this work is that of
parameter signature analysis and its application to failure mode pre-
diction.

A typical test of the readiness of an operational system is indi-
cated in Figure 2-5(b). This method is referred to as signal signature
analysis and typically consists of application of a step input $r(t)$ to
the system tested and observation of the system output $c(t)$ as sugges-
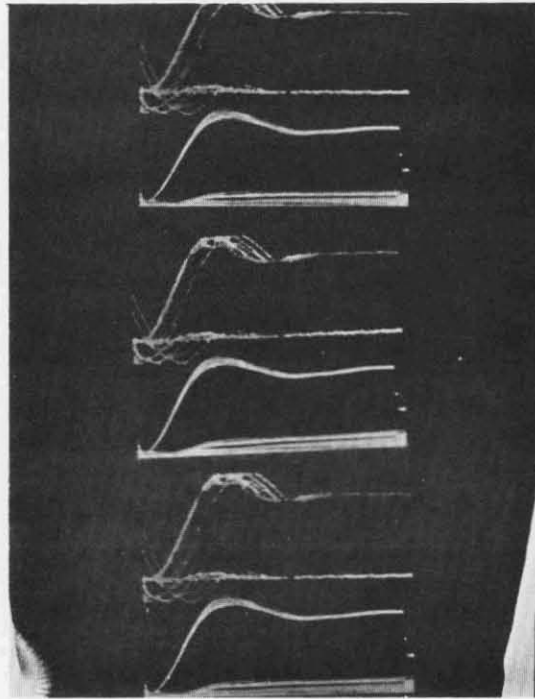
```
0 0 0 0 0 2 1 5
0 0 0 0 2 6 1 1
0 0 0 0 3 2 5 0
0 0 0 0 1 4 2 5
0 0 0 0 2 6 1 1
0 0 0 0 0 5 4 0
```

Figure 2-4   Physical Example-Position Servomechanism

(b)

(a)
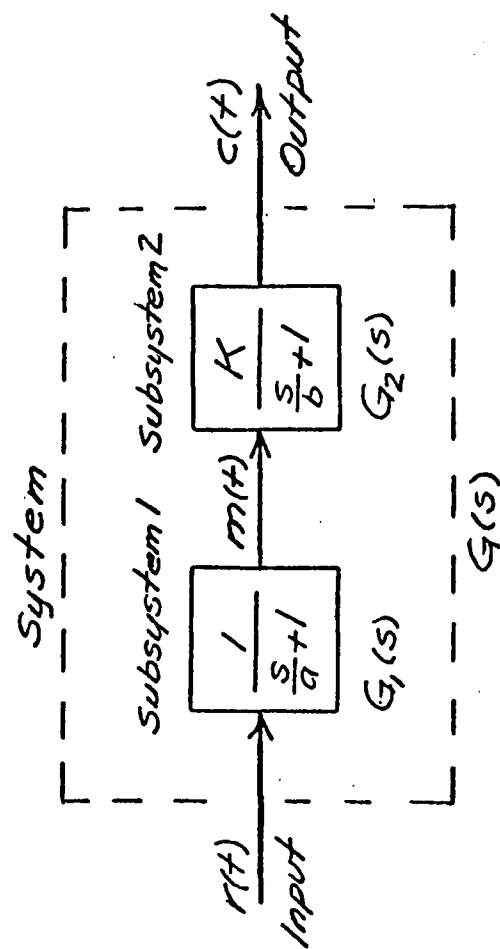
Figure 2-5 Signal Signature Analysis

tolerance limits on b

b_nominal

t in weeks →

Each point is obtained from a single test such as in Figure 2-5(b)

tolerance limits on a

a_nominal

t in weeks →

(c)

Figure 2-5 Parameter Signature Analysis

ted in Figure 2-5(a). The actual system c :put is compared with cer-
tain tolerance curves, either by the man making the decision or by a
machine providing the decision maker with data. Both experience and
analysis show that the decision process based on signal signature analy-
sis fails in certain reasonably simple, physically-occurring situations.
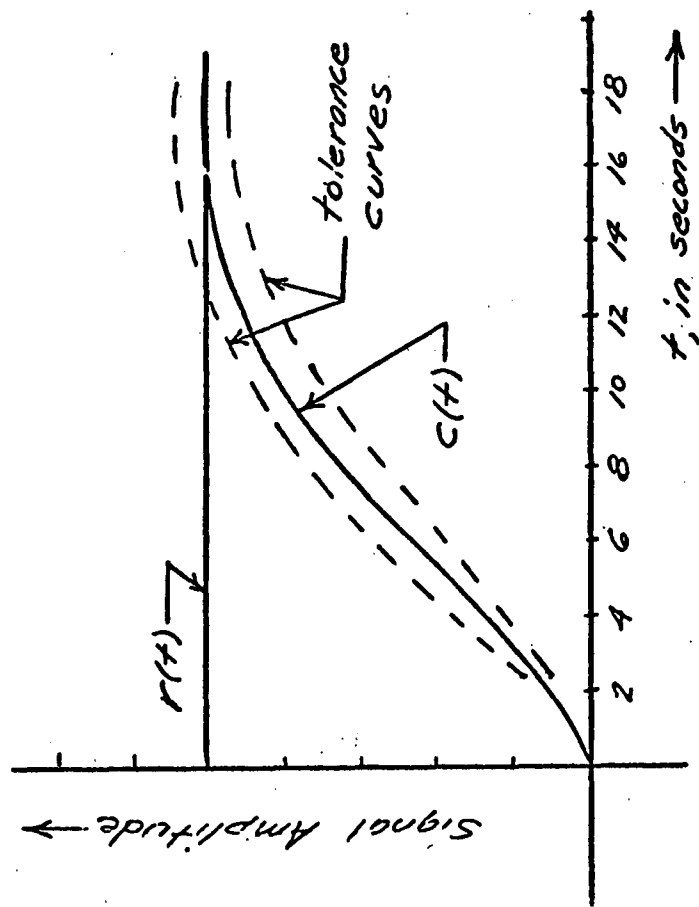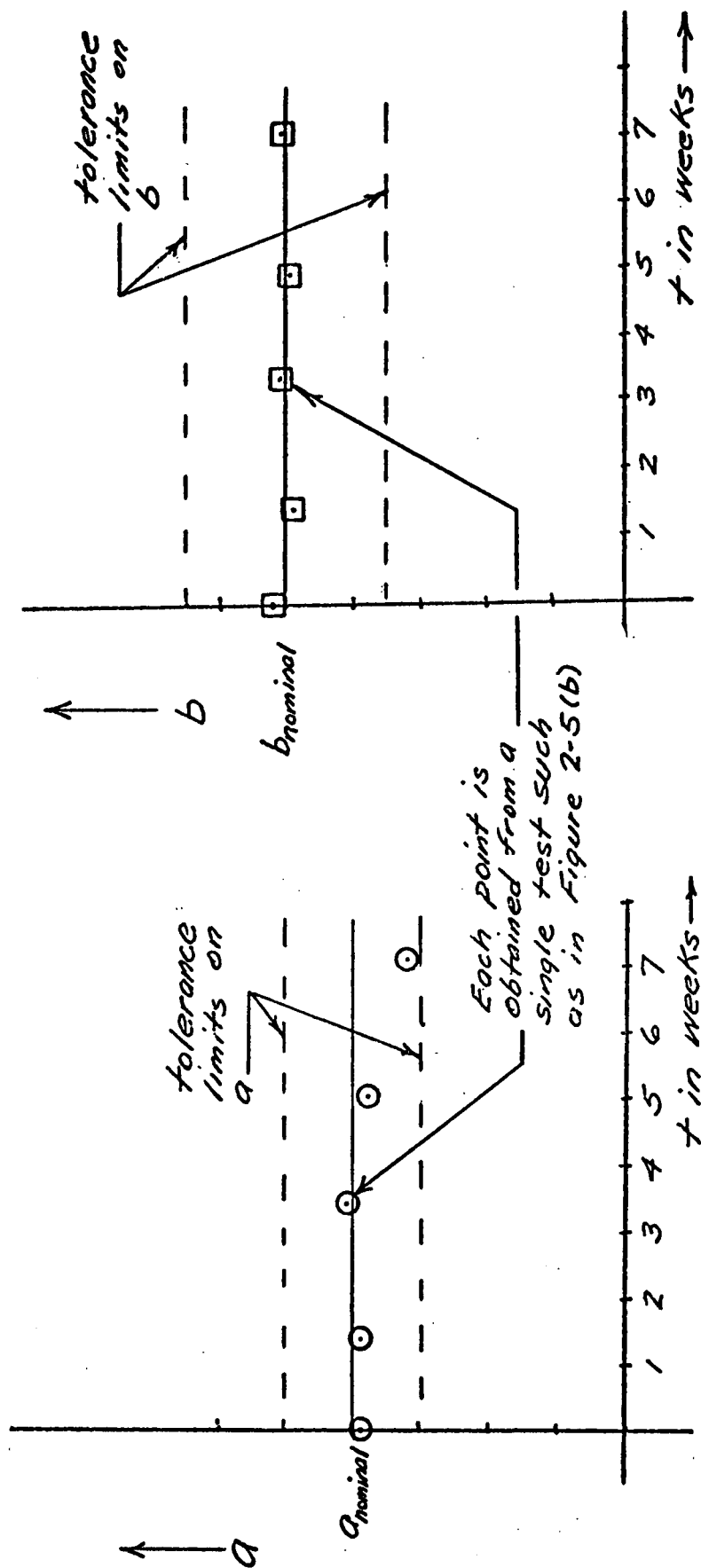For this reason, parameter signature analysis has been suggested as an
alternative to signal signature analysis.

The basic concept of parameter signature analysis is suggested in
Figure 2-5(c). The parameters of the system are identified at high
speed as previously described. The results of each identification
are plotted as single points (not functions) as shown in the para-
meter signatures of Figure 2-5(c). For quick-look analysis and de-
cisions on the present state of readiness of the system, the model
parameters must lie within pre-determined tolerance limits which can
be pre-determined from subsystem tests and specifications.

For failure prediction, long-term trends on the parameter signa-
ture plots are observed (note the time-scale difference between
Figures 2-5(b) and 2-5(c)). The decision to replace potentially de-
fective subsystems before complete failure can be based on long
term trends of the parameter signature towards an out-of-tolerance
comdition. In effect, the parameter signature can be time-scaled
to provide a history of the performance of the subsystems dating
from the acceptance test to the given operational test.

Experience with modeling in our laboratories indicates that
parameters may undergo relatively large changes with relatively little
obvious effect in the signal signatures. This suggests that parameter

trends are a better indication of degradation in sybsystem performance than are signal signatures. Typical test results which verify this idea are shown in Figure 2-6. These results are from a simple linear third-order dynamic system subjected to a step input, which simulates conditions in system readiness testing under operational conditions. The system transfer function for the linear system tested is

$$G(s) = \frac{p_1}{s^3 + p_2 s^2 + p_3 s + p_4}$$

(2.1)

In this test the parameter p_2 was changed slowly with all other parameters p_1 fixed and the resulting step responses observed as shown in Figures 2-6. There it is seen that with a change of $\frac{3}{18} = 17\%$ in p_2 the change in the corresponding signal signatures would be either un-detectable, or barely detectable, by a very alert human monitor. All of the signal signatures, corresponding to a parameter change of 50% in p_2, would probably fall within tolerance bounds for a typical readiness test as suggested in Figure 2-5(b). Using our techniques, a parameter change of 2-3% is typically detectable by processing the signal signatures and therefore the parameter signatures may be used to provide the human monitor with indications of system change that he would not obtain from typical signal signature analysis. The use of parameter signatures with parameter bounds can be easily automated to provide a "go-no go" indication to the human monitor as suggested in Figure 2-5(c).

The use of this idea in failure mode prediction is indicated by the test results of the next section. As previously explained,
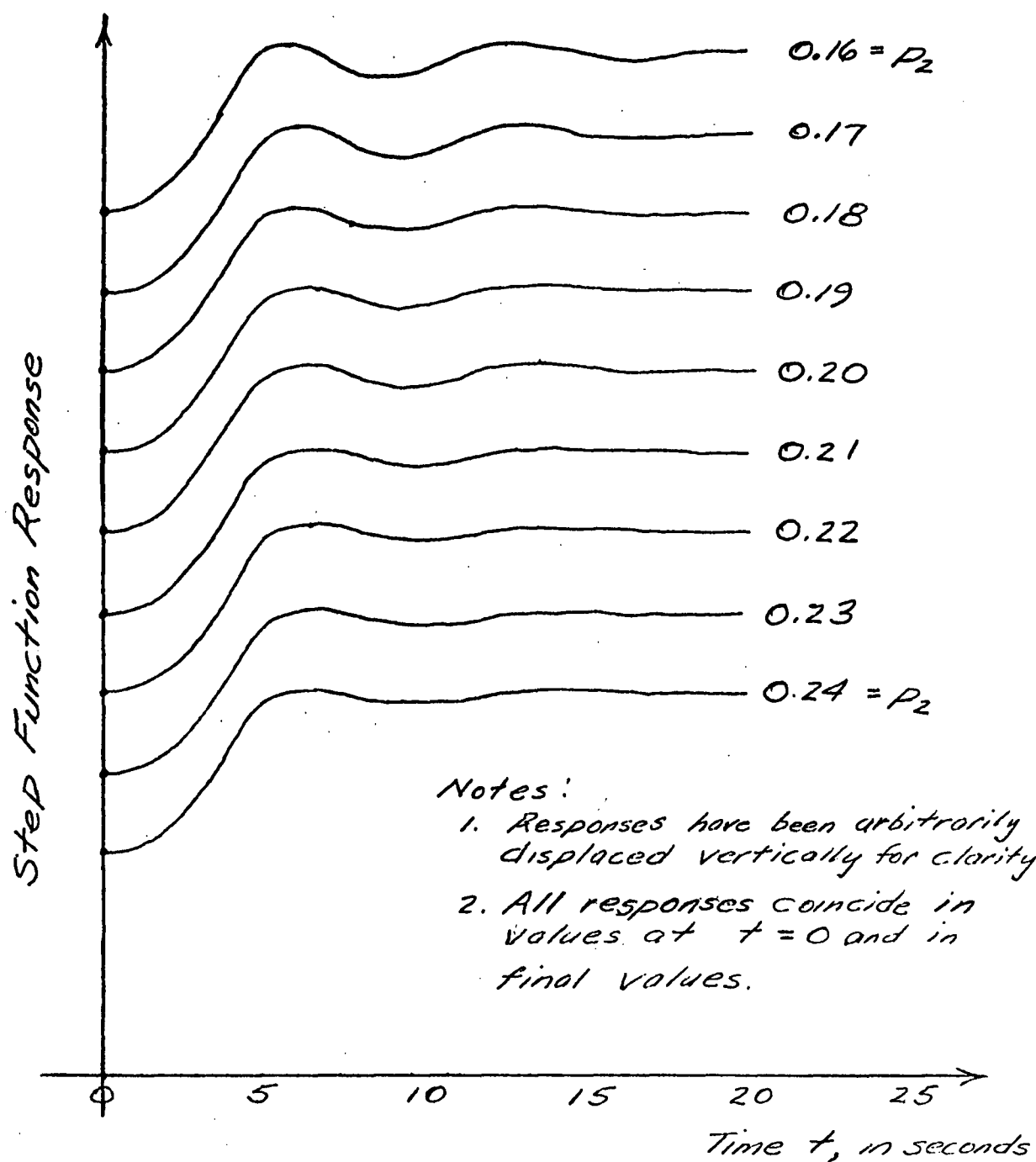
Figure 2-6 Demonstration of the Advantage of Parameter Signature
Analysis Over Signal Signature Analyser

the concept of failure mode prediction is basically different from

"go-no go" testing in that an attempt is made to detect trends towards

out-of-tolerance conditions before such conditions actually occur.

5). Failure Mode Prediction Results

The test results of Figure 2-7 provide a laboratory verification

of the failure mode prediction concept. The parameter estimates were

obtained from the step response of a linear system with transfer function

given by

$$G(s) = \frac{p_1}{s^3 + p_2 s^2 + p_1 s + p_4}$$

(2.2)

In the example shown in Figure 2-7(a), parameter p_3 was changed rather

abruptly and parameter p_2 was changed rather gradually. The trends

of the parameter estimates for both p_2 and p_3 indicate the nature

of the system changes that actually took place. Both the rapid change

in p_3 and the gradual drift of p_2 are correctly indicated. Either a

human or computer monitor could easily detect the approaching out-

of-tolerance condition for parameter p_2 in this case, although the

changes in the signal signatures are barely detectable and would fall

within typically acceptable tolerance limits as previously indicated.

Numerous other tests of similar nature have been made in the

laboratory, and these have been successful in general. However, it

has been discovered that the tracking of certain parameters in certain

systems may be considerably more difficult than tracking of other para-

meters. This appears to be a sensitivity, or a parameter scaling,

problem and this problem is not completely understood yet in its gen-

eral form. It is now believed that the solution may be related to distribution of the computational loop gain. For example, with a relatively insensitive parameter it may be desirable to increase the computational gain in Figure 2-1 from error $e(t)$ to performance index P to the parameter adjustment p_1 through the optimization program. It is believed that one of the basic advantages of using the Fletcher-Reeves or similar algorithm in this class of problems is that computational loop stability can be maintained at a higher computational gain for relatively insensitive parameters.

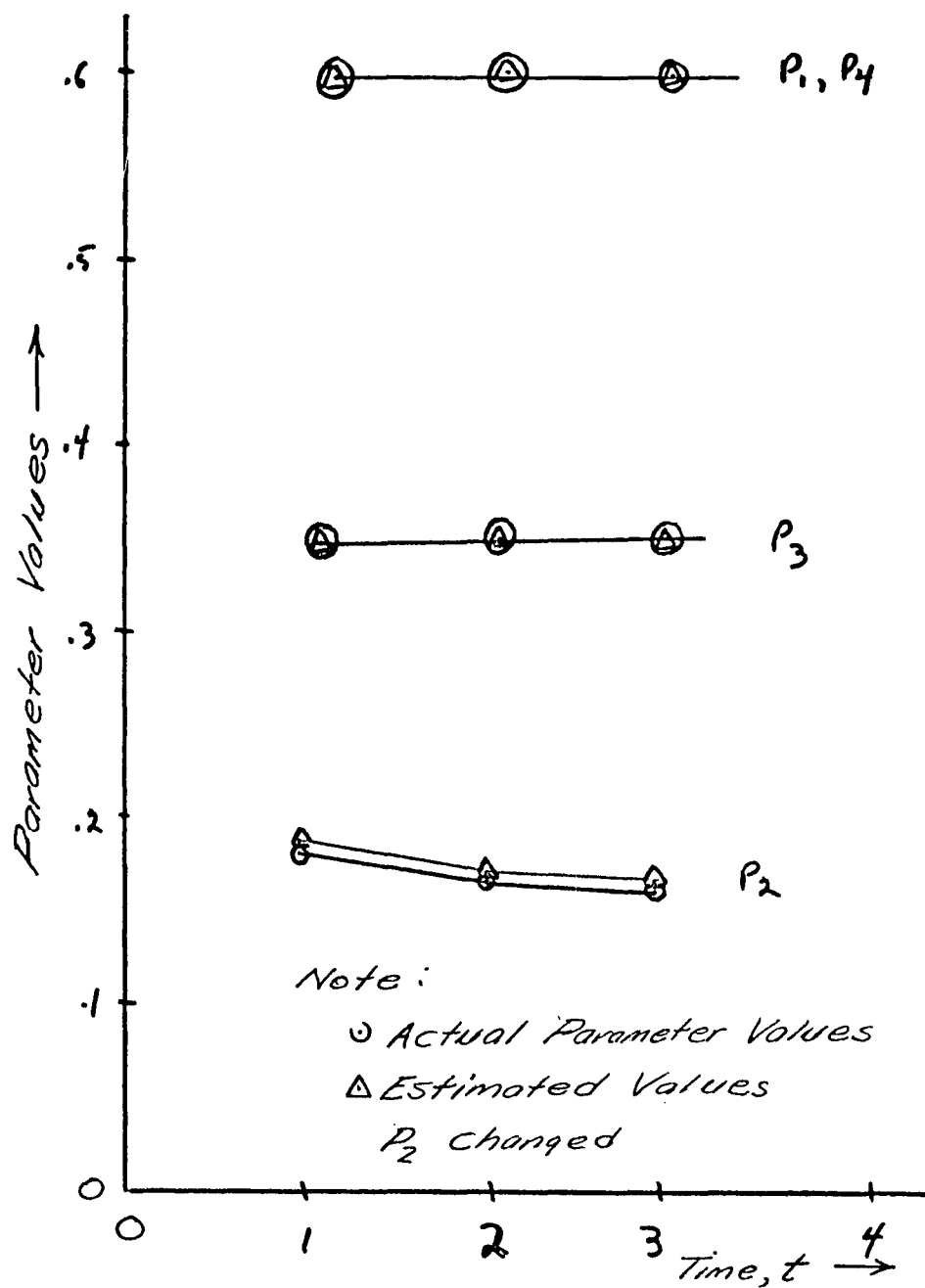Figure 2-7(a) Failure Mode Prediction Test Results.
Two Parameters Changing

Figure 2-7(b)   Failure Mode Prediction Test Results
One Parameter Changing

PART 3   DIGITALLY CONTROLLED NONLINEAR FUNCTION GENERATOR (DCNFG)

A.   Introduction and Motivation

The purpose of this part of the work was to allow a rather general nonlinear analog transmission characteristic to be generated under control of the digital computer as suggested by Figures 3-1 and 3-2.

The basic idea for the DCNFG arose from the need to extend the high-speed automated modeling technique to rather general <u>nonlinear</u> systems. The basic application of the technique had been previously investigated for some simple nonlinear systems [6,7]. These cases were necessarily simple because of limited digital control of the nonlinear analog components. Manual setting of the analog function generators took too much time and, of course, did not allow optimization of the nonlinearity under program control. Analog nonlinear operations were desired so that additional analog to digital (A/D) and digital to analog (D/A) conversions could be avoided. The initial concept of combining a digitally set potentiometer (DPU) with commercially available function generators was not implemented. A simpler improved design was conceived, constructed, debugged, and applied to nonlinear problems as described in the following sections of this part of the report.

B.   DCNFG Design and Implementation

1).   Description of Nonlinearity to be Realized

Figure 3-1 schematically describes an analog computer component, the DCNFG, which has a V_{out} vs. V_{in} characteristic that in nonlinear. The shape of this nonlinearity is controlled by the digital words received at the digital input terminal of this device.

A typical V_{out} vs. V_{in} characteristic achievable with the DCNFG designed and constructed is shown in Figure 3-2. The V_{in} and V_{out} ranges

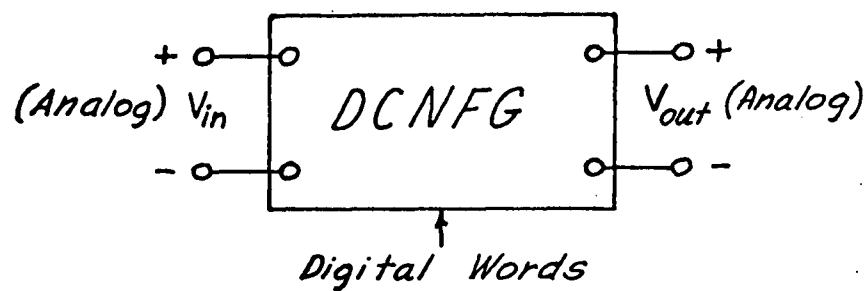Figure 3-1   The Digitally Controlled Nonlinear
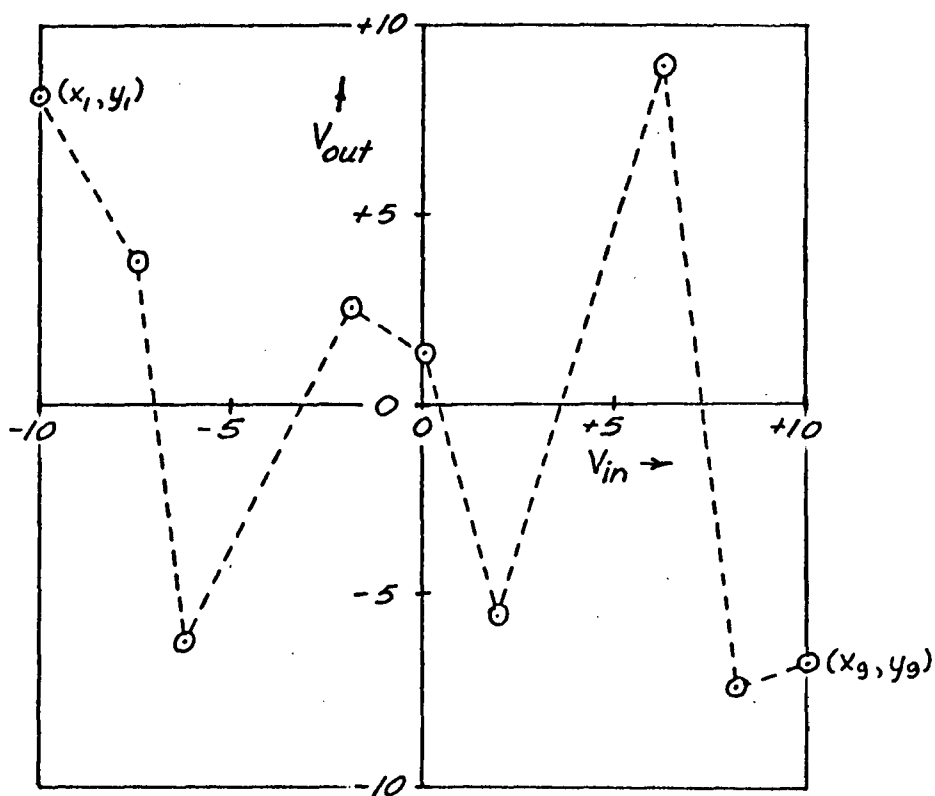Function Generator

Figure 3-2   Voltage Transfer Characteristic of
the DCNFG

of the device are each $\overset{+}{-}$ 10 volts. The characteristic is composed of eight straight line segments or sections and a complete characteristic can be described by the x (V_{in}) and y (V_{out}) coordinates of the nine points on the characteristic. The leftmost point is (x_1, y_1) and the rightmost point is (x_9, y_9), with the x coordinates satisfying the inequality relationship

$$-10 \overset{\le}{-} x_1 < x_2 < x_3 < x_4 < x_5 < x_6 < x_7 < x_8 < x_9 \overset{\le}{-} 10 \tag{3.1}$$

The digital inputs indicated in Figure 3-1 control the positions of these nine points on the transfer characteristic.

Figure 3-3 shows a detailed diagram of one arbitrary section, section I, of the nonlinear characteristic. For the eight section DCNFG, $1 \overset{\le}{-} I \overset{\le}{-} 8$. The defining equations for the three parameters V_{IO}, ΔV_I, and ΔH_I associated with section I in terms of the end point coordinates (x_I, y_I) and (x_{I+1}, y_{I+1}) of the section are

$$V_{IO} = \frac{x_{I+1} + x_I}{2} \tag{3.2}$$

$$\Delta V_I = x_{I+1} - x_I \tag{3.3}$$

$$\Delta H_I = y_{I+1} - y_I \tag{3.4}$$

Notice that V_{IO} is the x coordinate of the midpoint, that ΔV_I is always positive, and that ΔH_I takes on the algebraic sign of the slope of the
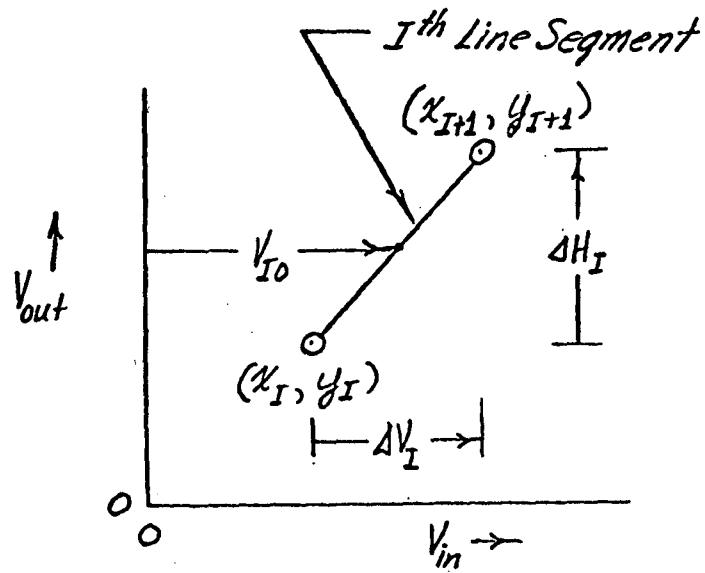
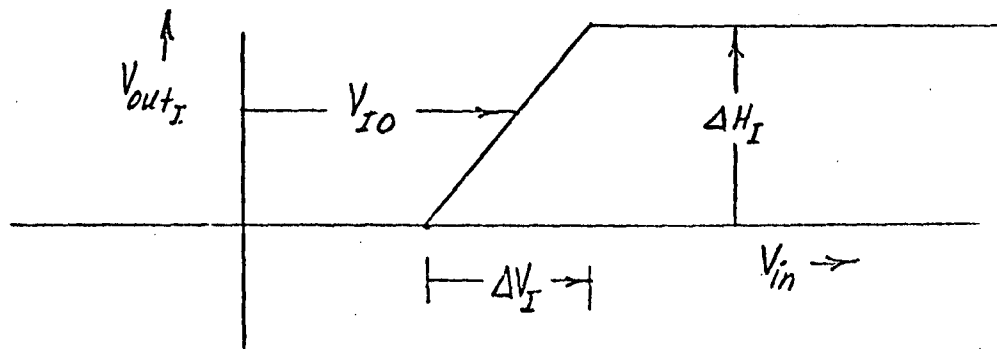Figure 3-3 Parameters Describing Section I of the
Nonlinear Characteristic

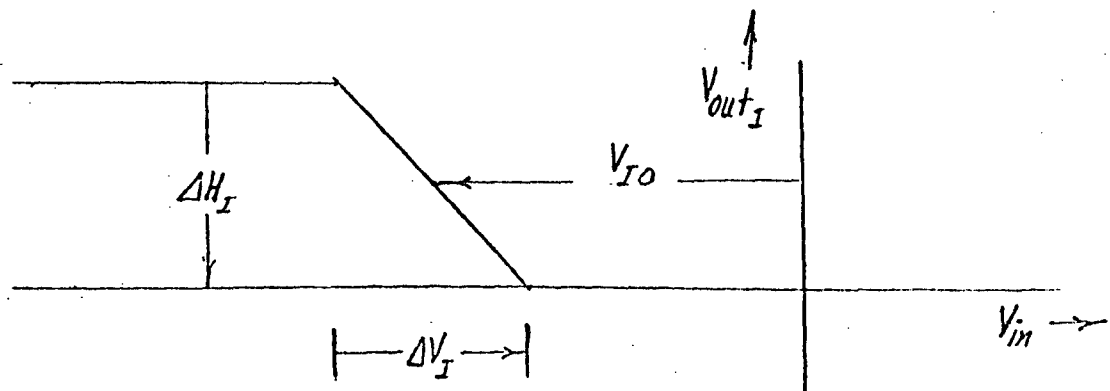Figure 3-4A A Right Hand Function

Figure 3-4B A Left Hand Function

I^{th} line segment.

2). Synthesis of Nonlinearity

The actual realization or synthesis of the eight section nonlinearity is accomplished as follows. Eight individual functions of the two types shown in Figures 3.4A and 3.4B are first generated. The right hand function of Figure 3.4A has $V_{out} = 0$ for all $V_{in} \leq x_I$, while the left hand function has $V_{out} = 0$ for all $V_{in} > x_{I+1}$. If V_{IO} is positive or zero, a right hand function is generated. If V_{IO} is negative a left hand function is generated in this synthesis procedure. The synthesis procedure is completed by adding the above eight functions to the constant function $V_{out} = V_{LEVEL}$ where V_{LEVEL} is the y_I coordinate of the section having the smallest nonnegative V_{IO} value. See Figure 3.5 for a graphical presentation of this adding or "building up" process.

In Figure 3-5 the three dotted functions are left hand functions, the three dashed functions are right-hand functions, and the dash-dot line is V_{LEVEL}. The solid line is the sum of these seven functions and shows the "building up" process taking place.

3). Analog Circuit Realization of One Segment of the Nonlinear Function

The analog computer diagram shown in Figure 3-6 is a realization of either a right-hand or a left-hand $(V_{out})_I$ vs V_{in} characteristic. The voltage transfer characteristic of this operational amplifier circuit is controlled by the three variable (digitally-controlled) resistors R_{IO}, $R_{\Delta V}$, and $R_{\Delta H}$, and by the three digitally controlled switches SW1, SW2, and SW3. Three eight bit digital words, word V_{IO}, word ΔV_I, and word ΔH_I, control the above six circuit elements as follows. Switches
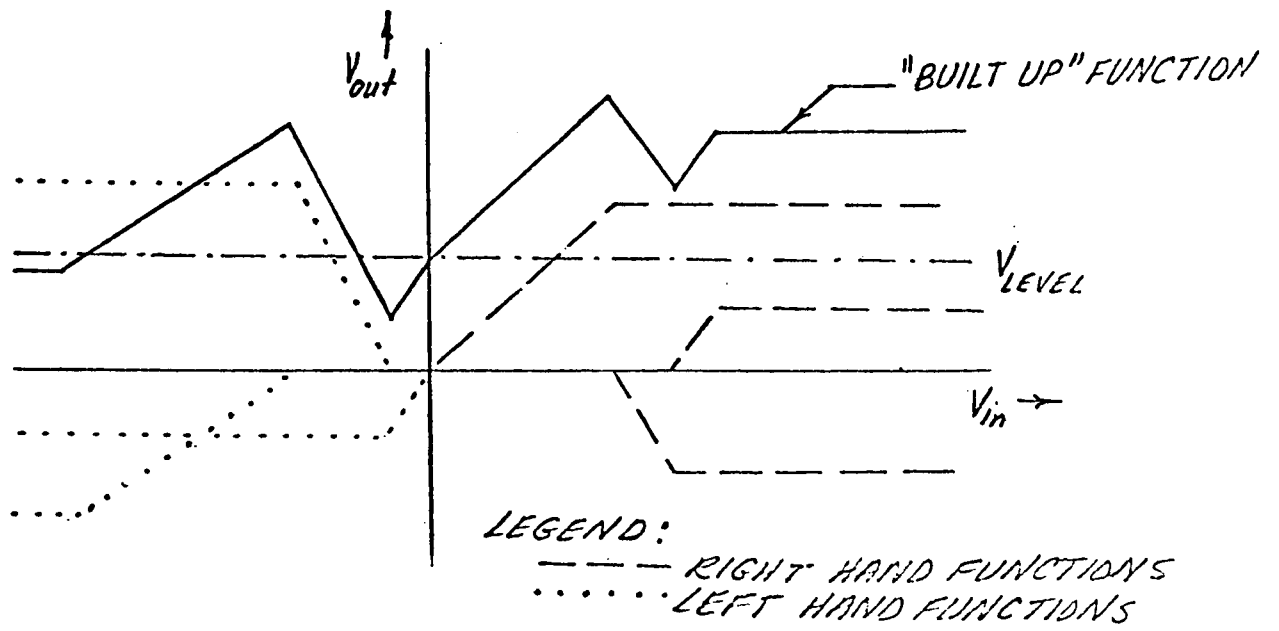
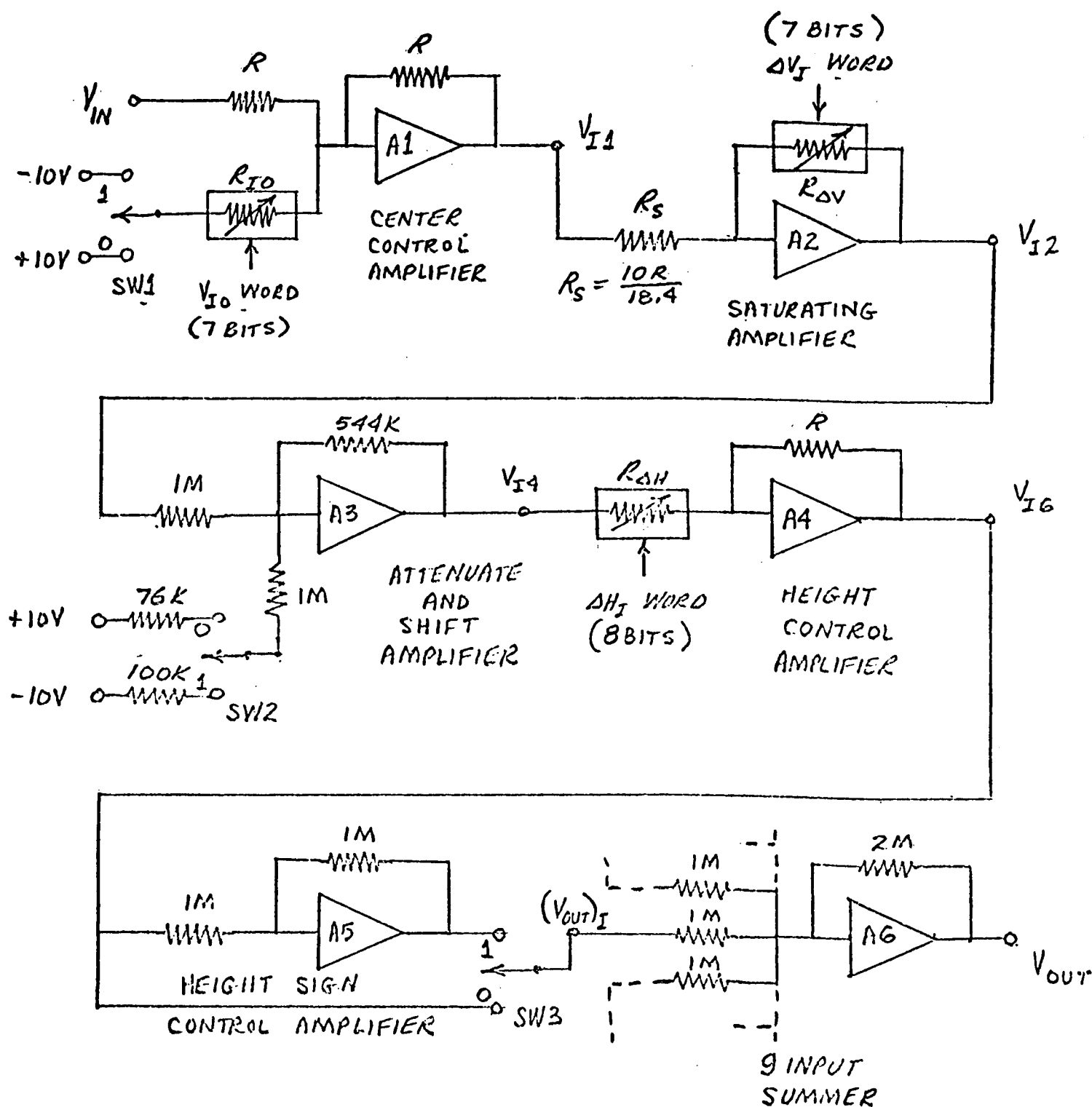Figure 3-5 Synthesis of the Nonlinear Function

Figure 3-6 Analog Computer Realization of One Section
of Variable Break Point DCNFG

SW1 and SW2 are controlled by the most significant bit (or sign bit) of the word V_{IO}. Switch SW3 is controlled by the most significant bit of the word ΔV_I. Resistor R_{IO} is controlled by the remaining seven bits of word V_{IO} and resistor $R_{\Delta V}$ by the remaining seven bits of word ΔV_I. Resistor $R_{\Delta H}$ is controlled by the eight bits of word ΔH_I.

The block diagram of Figure 3-7 shows how the resistor $R_{\Delta H}$ is controlled by the eight bit work ΔH_I. Let the word ΔH_I be represented by the word ABCDEFGH where A = 0 or 1, B = 0 or 1, etc. In Figure 3-7 the buffer register stores the word ΔH_I. The digitally controlled FET switches represented schematically in this diagram are closed when the binary input to the switch is a "1" and open when the input is a "0". These FET switches connect and disconnect binarily weighted resistors R through 128R to and from the resistive "ladder" network. Therefore the resistance seen looking into terminals ab of this network consists of various parallel combinations of ladder resistors depending on the buffered word ΔH_I. The value of the conductance G_{ab} seen looking into terminals ab is therefore described by the equation

$$G_{ab} = \frac{1}{R_{ab}} = \frac{1}{R} \left[A + \frac{B}{2} + \frac{C}{4} + \frac{D}{8} + \frac{E}{16} + \frac{F}{32} + \frac{G}{64} + \frac{H}{128} \right] \quad (3.5)$$

The resistance R_{ab} will be used as resister $R_{\Delta H}$ in the circuit of Figure 3-6. Similar seven bit ladders will be used to generate the digitally controlled resistances R_{IO} and $R_{\Delta V}$.
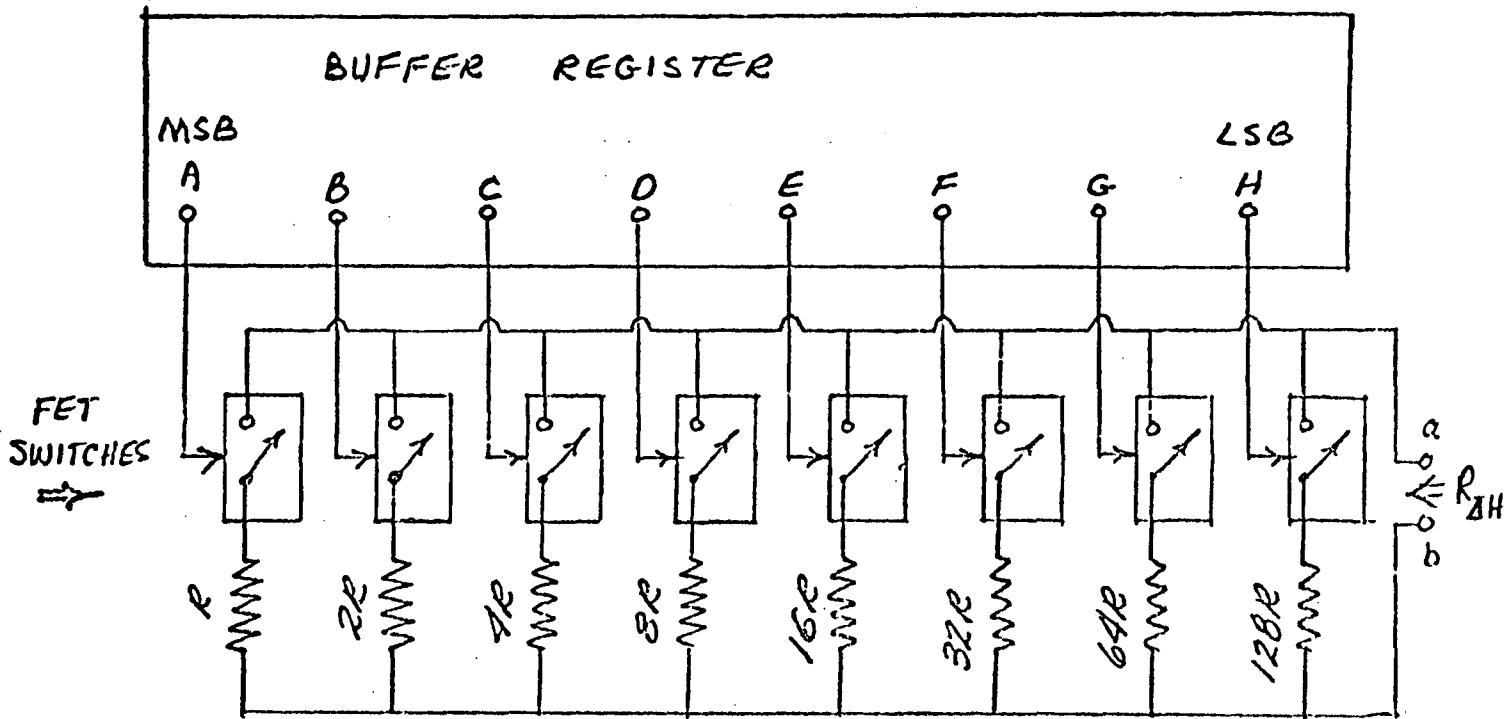
Figure 3-7 An Eight Bit Digitally Controlled Conductance
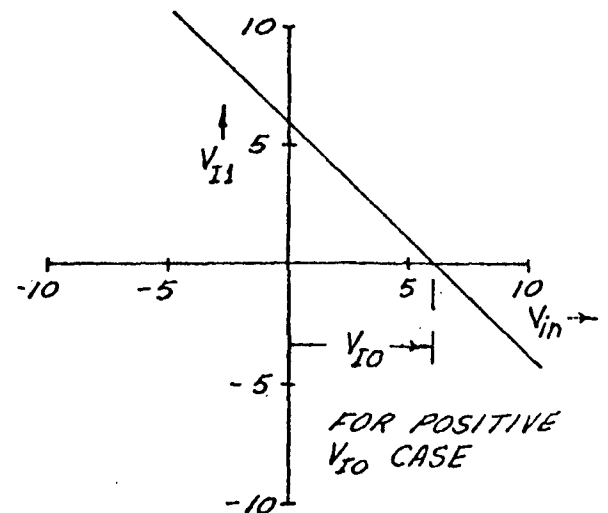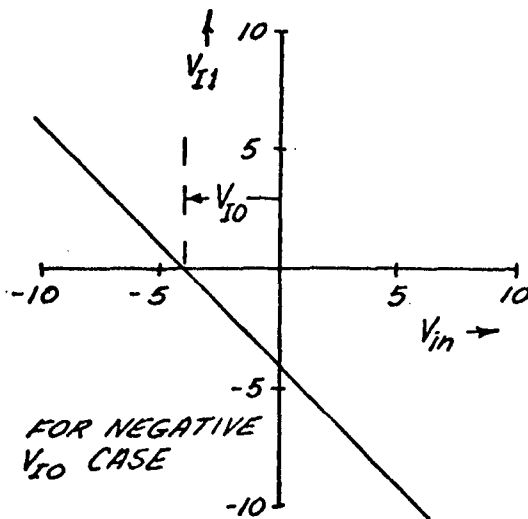
Figure 3-8 Voltage Transfer Characteristic of the
Center Control Amplifier

The following is a stage by stage description of how the operational amplifier circuitry of Figure 3-6 generates the desired right-hand and left-hand functions and how the shapes of these functions are controlled by the three eight-bit digital words V_{IO}, ΔV_I, and ΔH_I.

4). The Center Control Stage

The first stage of Figure 3-6 contains the center control amplifier A1. The voltage transfer function of this stage is described by the equation

$$V_{I1} = -(V_{in} - V_{IO})$$

(3.6)

where $|V_{IO}|$ is digitally controlled through the variable conductance of R_{IO} and the sign of V_{IO} is controlled by SW1. For this circuit it is easily shown that

$$V_{I1} = -\left(\frac{R}{R}\right) V_{in} \pm \left(\frac{R}{R_{IO}}\right) 10$$

(3.7)

Let the eight bit word V_{IO} be $A_o B_o C_o D_o E_o F_o G_o H_o$. Since the last seven bits control R_{IO} using a ladder network identical to that shown in Figure 3-7 with resistor R disconnected, then

$$G_{IO} = \frac{1}{R_{IO}} = \frac{1}{2R}\left[B_o + \frac{C_o}{2} + \frac{D_o}{4} + \cdots + \frac{H_o}{64} \right]$$

(3.8)

The most significant bit, A_o, controls the sign of V_{IO} by digitally controlling the single pole double throw FET switch SW1. When A_o is a "1", V_{IO} is positive, and SW1 is connected to the -10V supply. When A_o is a "0", V_{IO} is negative, and SW1 is connected to the +10V supply.

Therefore

$$V_{IO} = (2A_o - 1)(\frac{10\,R}{R_{IO}})$$ (3.9)

$$V_{IO} = (2A_o - 1)(5)(B_o + \frac{C_o}{2} + \cdots + \frac{H_o}{64})$$ (3.10)

The above eight bit coding scheme yields maximum and minimum V_{IO} magnitudes of $|V_{IO}|_{min} = 0$ volts and $|V_{IO}|_{max} = 9.922$ volts.

The smallest increments in V_{IO} are $\Delta V_{IO} = 5/64 \doteq 0.078$ volts. Table 3-1 lists the major binary to analog conversion points for this coding scheme.

Figure 3-8 shows, in graphical form, the voltage transfer characteristic of the center control amplifier stage for both positive and negative V_{IO} situations.

5). The Saturating Amplifier Stage

The second stage of Figure 3-6 contains the saturating amplifier A2. Amplifier A2 is powered from a $\pm$ 10.0 volt supply and saturates at +9.3 volts and -9.1 volts. Amplifiers A1, A3, A4, A5, and A6 are powered from a $\pm$ 15 volt supply and saturate at about $\pm$ 14 volts. The voltage transfer characteristic of the saturating amplifier stage is shown in Figure 3-9.

The linear gain for this stage is, from the circuit of Figure 3-6, described by

$$(GAIN)_{A2} = \frac{\Delta V_{I2}}{\Delta V_{I1}} = \frac{-R_{\Delta V}}{R_s}$$ (3.11)

From Figure 3-9 the linear gain of this stage is

$$(GAIN)_{A2} = \frac{\Delta V_{I2}}{\Delta V_{I1}} = \frac{-(9.3 + 9.1)}{\Delta V_I}$$ (3.12)

8 Bit Word V_{IO}	Analog Voltage V_{IO}	8 Bit Word V_{IO}	Analog Voltage V_{IO}
01000000	-5.000V	11000000	+5.000V
00100000	-2.500V	10100000	+2.500V
00010000	-1.250V	10010000	+1.250V
00001000	-0.625V	10001000	+0.625V
00000100	-0.312V	10000100	+0.312V
00000010	-0.156V	10000010	+0.156V
00000001	-0.078V	10000001	+0.078V
00000000	-0.000V	10000000	+0.000V
01111111	-9.922V	11111111	+9.922V

Table 3-1 Binary to Analog Conversion Chart for V_{IO}

Last 7 Bits of Word ΔV_I	Value of ΔV_I	Last 7 Bits of Word ΔV_I	Value of ΔV_I
1000000	5.000V	0000010	0.156V
0100000	2.500V	0000001	0.078V
0010000	1.250V	0000000	0.000V
0001000	0.625V	1111111	9.922V
0000100	0.312V		

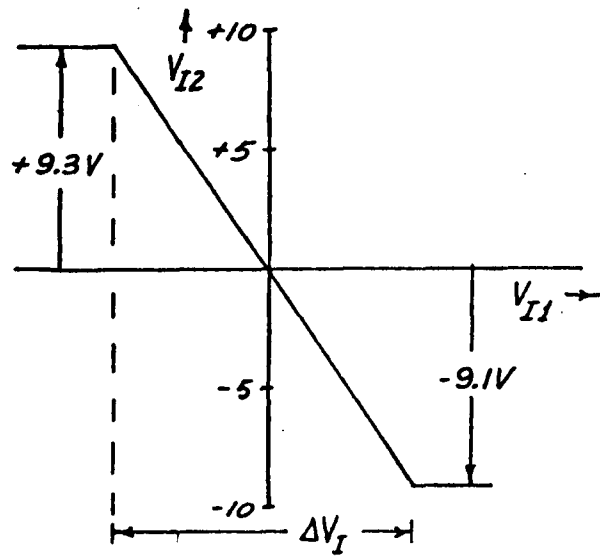Table 3-2 Binary to Analog Conversion Chart for ΔV_I

Figure 3-9   Voltage Transfer Characteristic of the
Saturating Amplifier
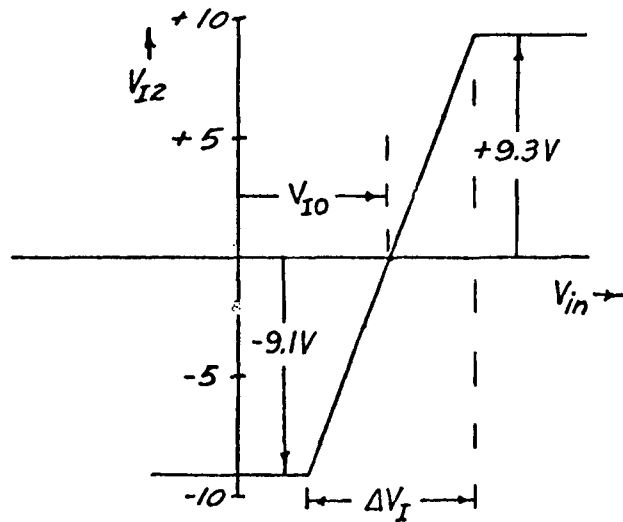
Figure 3-10   Voltage Transfer Characteristic of
The First Two Stages

Therefore

$$V_I = (18.4)(R_s/R_{\Delta V})$$ (3.13)

and for a fixed R_s the digitally controlled resistor $R_{\Delta V}$ controls
the value of ΔV_I.

If the eight bit word V is $A_v B_v C_v D_v E_v F_v G_v H_v$ and if the last seven bits
are used to control the value of $R_{\Delta V}$ (once again using the circuit of
Figure 3-7 with resistor R removed) then

$$G_{\Delta V} = \frac{1}{R_{\Delta V}} = \frac{1}{2R}\left[B_v + \frac{C_v}{2} + \frac{D_v}{4} + \cdots + \frac{H_v}{64} \right]$$ (3.14)

A binary coding of ΔV_I similar to the coding of V_{IO} is desired and is
attained by setting

$$\Delta V_I = 5\left[B_v + \frac{C_v}{2} + \frac{D_v}{4} + \cdots + \frac{H_v}{64} \right]$$ (3.15)

yielding only non-negative ΔV_I values, as required, and resulting in
a maximum ΔV_I value of

$$(\Delta V_I)_{max} = 5\left[1 + \frac{63}{64} \right] \doteq 9.222 \text{ volts}$$ (3.16)

The smallest increments in ΔV_I are $5/64 \doteq 0.078$ volts. Table 3-2 lists
the major binary and analog conversion points for this coding scheme.
From this coding scheme it is obvious that ΔV_I must equal 5.00 volts
when $R_{\Delta V} = 2R$ since this is the only ladder resistor switched in when
the word ΔV_I has $B_v C_v D_v E_v F_v G_v H_v = 1000000$. Using this data point, the

required value of R can be determined using Equation (3.13) and is

$$R_s = \frac{R_{\Delta V} \Delta V_I}{18.4} = \frac{2R \ (5)}{18.4} = \frac{10R}{18.4} \qquad (3.17)$$

Figure 3-10 shows the overall voltage transfer characteristic for

the first two stages when V_{IO} is positive.

6). The Attenuate and Shift Stage

The third stage of Figure 3-6 contains the attenuate and shift amplifier

A3. The purpose of this amplifier is to produce the pair of V_{I4} vs V_{in}

characteristics shown in Figure 3-11 corresponding to the pair of sit-

uations $V_{IO} \geq 0$ and $V_{IO} < 0$.

These characteristics are attained by attenuating and shifting the voltage

V_{12}. Since A2 saturates at +9.3 volts and -9.1 volts and since a dif-

ference of 10 volts is desired between the saturation levels (caused

by A2) present at the output of A3, the gain of stage A3 must be

$$(GAIN)_{A3} = \frac{\Delta V_{I4}}{\Delta V_{I2}} = \frac{-10.0}{9.3 + 9.1} = -0.544 \qquad (3.18)$$

This $(GAIN)_{A3}$ scales the 9.3 volt saturation level to -5.054 volts and

the -9.1 volt level to +4.946 volts. That is, if SW2 were opened the

V_{I4} vs. V_{in} characteristic would have the shape shown in Figure 3-12.

To attain the right hand characteristic of Figure 3-11 the characteris-

tic of Figure 3-12 must be shifted "up" 5.054 volts by switching SW2

to the -10 volt (100 k ohm) position since

$$(-10 \text{ volts}) \ (\frac{-544 \text{ k ohm}}{1000 \text{ k ohm} + 100 \text{ k ohm}}) = +5.054 \text{ volts}$$
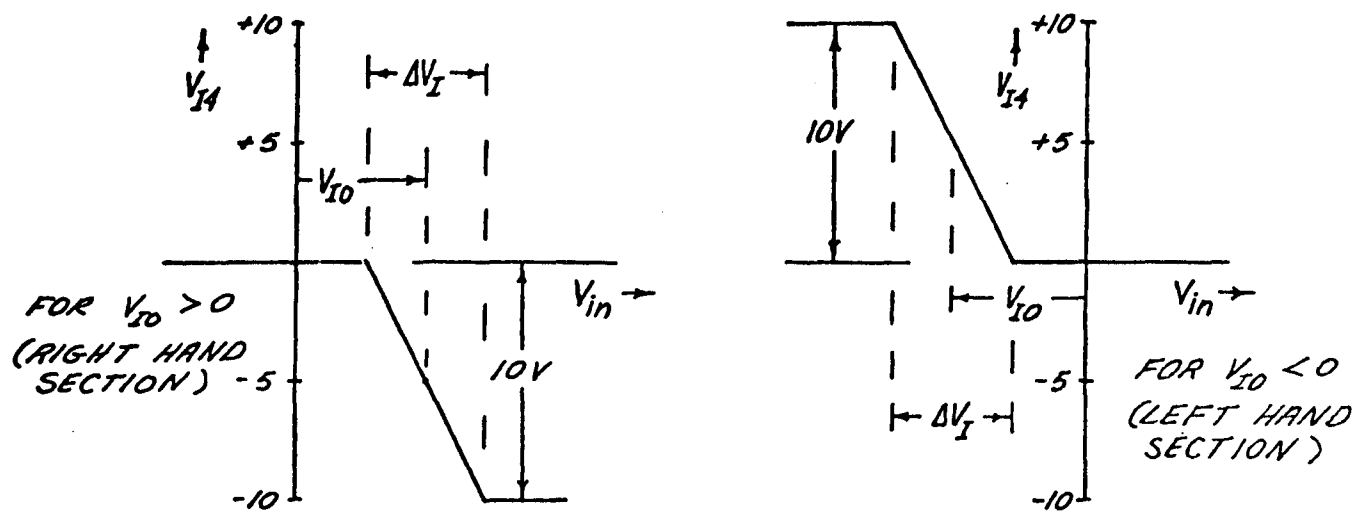
$$(3.19)$$

Figure 3-11   Voltage Transfer Characteristic of
The First Three Stages
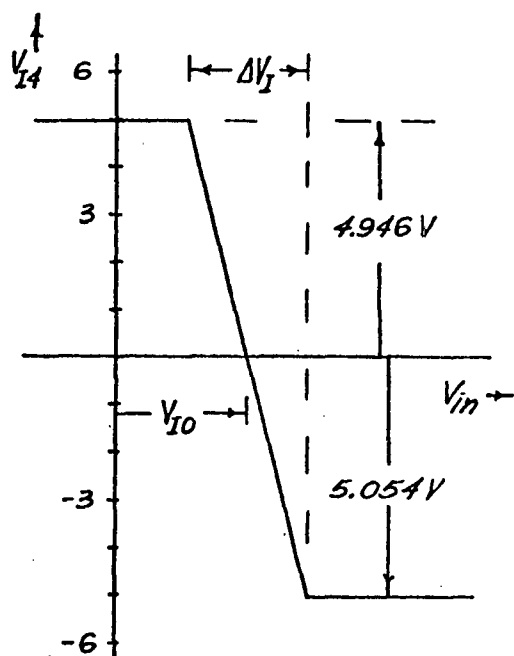
Figure 3-12   Voltage Transfer Characteristic of the
First Three Stages When SW2 Is Open

Since a right hand characteristic is desired when V_{IO} is non-negative, the sign control bit A_o of the word V_{IO} is used to control SW2. When A_o is a "1" SW2 is connected to the -10 volt position.

To attain the left hand characteristic of Figure 3-11 the characteristic of Figure 3-12 must be shifted "down" 4.946 volts by switching SW2 to +10 volt (76 k ohm) position since

$$(+10 \text{ volts}) \left(\frac{-544 \text{ k ohm}}{1000 \text{ k ohm} + 76 \text{ k ohm}} \right) = -4.946 \text{ volts}$$

(3.20)

Since a left hand characteristic is desired when V_{IO} is negative, SW2 is connected to the +10 volt position when A_o is a "0".

7). The Height Control Stage

The fourth stage of Figure 3-6 contains the height control amplifier A4. The operation of A4 is very similar to the operation of A1. The gain of A4 is

$$(GAIN)_{A4} = \frac{\Delta V_{I6}}{\Delta V_{I4}} = - \frac{(R/2)}{R_{\Delta H}}$$

(3.21)

If the eight bit word ΔH_I is $A_H B_H C_H D_H E_H F_H G_H H_H$ and the full eight bit ladder of Figure 3-7 is used then

$$G_{\Delta H} = \frac{1}{R_{\Delta H}} = \frac{1}{R} \left[A_H + \frac{B_H}{2} + \frac{C_H}{4} + \cdots + \frac{H_H}{128} \right]$$

(3.22)

and

$$(GAIN)_{A4} = - \frac{1}{2} \left[A_H + \frac{B_H}{2} + \frac{C_H}{4} + \cdots + \frac{H_H}{128} \right]$$

(3.23)

Since the ΔH present at point V_{14}, the input of A4, is always -10 volts, as is obvious from Figure 3-11, then the ΔH value present at the output of A4, at point V_{I6}, is ΔH_{I6} where

$$\Delta H_{I6} = -10 \; (\text{GAIN})_{A4} \tag{3.24}$$

and the maximum magnitude of ΔH_{I6} is

$$(\Delta H_{I6})_{max} = (10)(\frac{1}{2})(1 + \frac{127}{128}) \doteq 9.96 \text{ volts} \tag{3.25}$$

with incremental values of ΔH_{I6} of $5/128 \doteq 0.039$ volts.

Since the gain of A5 is ± 1.00 and the gain of A6 is -2.00,

$$\Delta H_I = \pm 2.00 \; \Delta H_{I6} \tag{3.26}$$

Therefore $(\Delta H_I)_{max} = 19.92$ volts and the smallest increment in ΔH_I is $5/64 \doteq 0.078$ volts. See Table 3-3.

8). Height Sign Control and Summer Stages

The fifth stage of Figure 3-6 contains inverting amplifier A5 and the height sign control switch SW3. Switch SW3 and as a result the sign of ΔH_I is controlled by the most significant bit, A_v, of the word ΔV_I. The sixth stage of Figure 3-6, A6, is a nine input inverting summer with a gain of -2.00. Therefore, when SW3 is connected to the output of A5 the ΔH_I present at the output of A6 is positive since ΔH_{I6} was positive and two inverters are connected between ΔH_{I6} and the output ΔH_I for this SW3 position. Since the coding A_v a "1" corresponds to ΔH_I positive is desired, then SW3 is connected to the output of amplifier

Sign Bit From ΔV_I	8 Bit Word ΔH_I	Value of ΔH_I	Sign Bit From ΔV_I	8 Bit Word ΔH_I	Value of ΔH_I
0	10000000	-10.000V	0	10000000	+10.000V
0	01000000	- 5.000V	0	01000000	+ 5.000V
0	00100000	- 2.500V	0	00100000	+ 2.500V
0	00010000	- 1.250V	0	00010000	+ 1.250V
0	00001000	- 0.625V	0	00001000	+ 0.625V
0	00000100	- 0.312V	0	00000100	+ 0.312V
0	00000010	- 0.156V	0	00000010	+ 0.156V
0	00000001	- 0.078V	0	00000001	+ 0.078V
0	00000000	-19.922V	0	11111111	+19.922V

Table 3-3 Binary to Analog Conversion Chart for ΔH_I

A5 when A_V is a "1". When A_V is a "0", SW3 is connected to the output of A4 and Equations 3.26, 3.24, and 3.23 can be combined and adjusted to account for the sign control bit A_V to obtain the expression

$$\Delta H_I = (2A_V - 1)(10)(A_H + \frac{B_H}{2} + \cdots + \frac{H_H}{128})$$

$$(3.27)$$

9). The Level Control Stage

Eight of the nine inputs of stage A6 are five stage sections identical to those shown in Figure 3-6. The ninth input to stage A6 is the level control signal. This signal is obtained from a single stage similar to stage A_1. See Figure 3-13.

An eight bit word $V_{LEVEL} = A_L B_L C_L D_L E_L F_L G_L H_L$ controls both the sign and magnitude of V_{LEVEL} according to the following expression.

$$V_{LEVEL} = (2A_L - 1)(5)(B_L + \frac{C_L}{2} + \frac{D_L}{4} + \cdots + \frac{H_L}{64})$$

$$(3.28)$$

if switch SW4 is connected to the +10V position when A_L is a "1" and connected to the -10V position when A_L is a "0". Therefore V_{LEVEL} has a maximum value of 9.922 volts with increments of 0.078 volts. The coding is identical to the V_{IO} coding of Table 3-1.

10). Description of Design Implementation

Figure 3-14 shows in block diagram form how the digital control of the conductance G_{IO}, $G_{\Delta V}$, and $G_{\Delta H}$ and hence the shape of the nonlinear characteristic was controlled by a sequence of 14 bit outputs from the Athena digital computer. The 8 bit output register A-H is connected in parallel to 25 eight bit storage registers ($8V_{IO}$ registers, $8\Delta V_I$ registers, $8 \Delta H_I$ registers, and 1 V_{LEVEL} register). These 25 registers
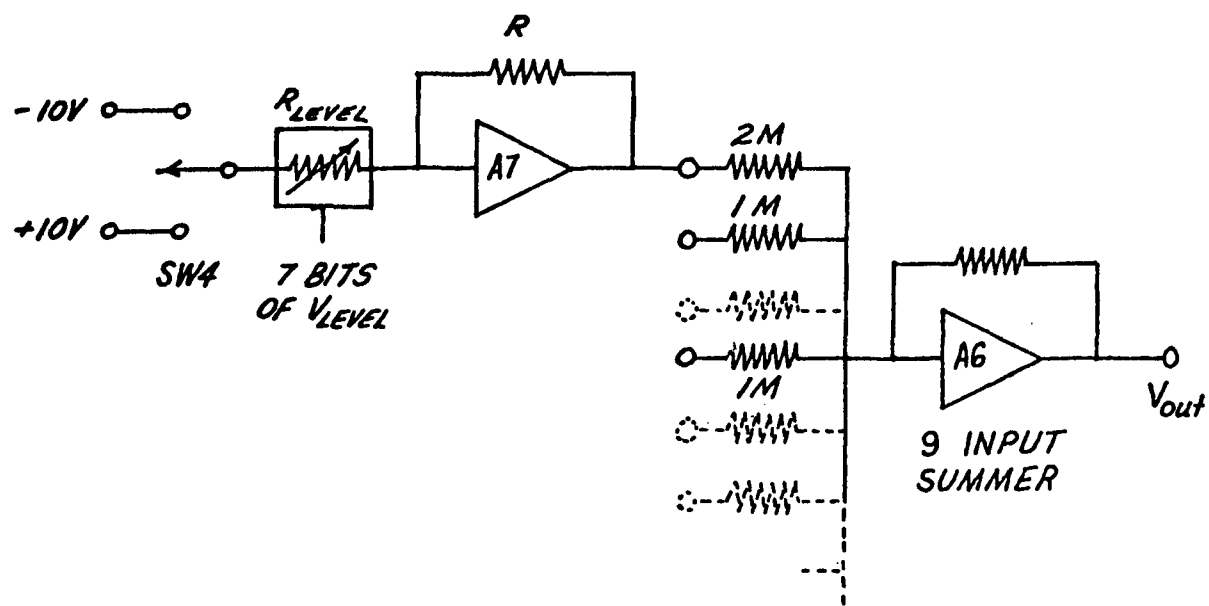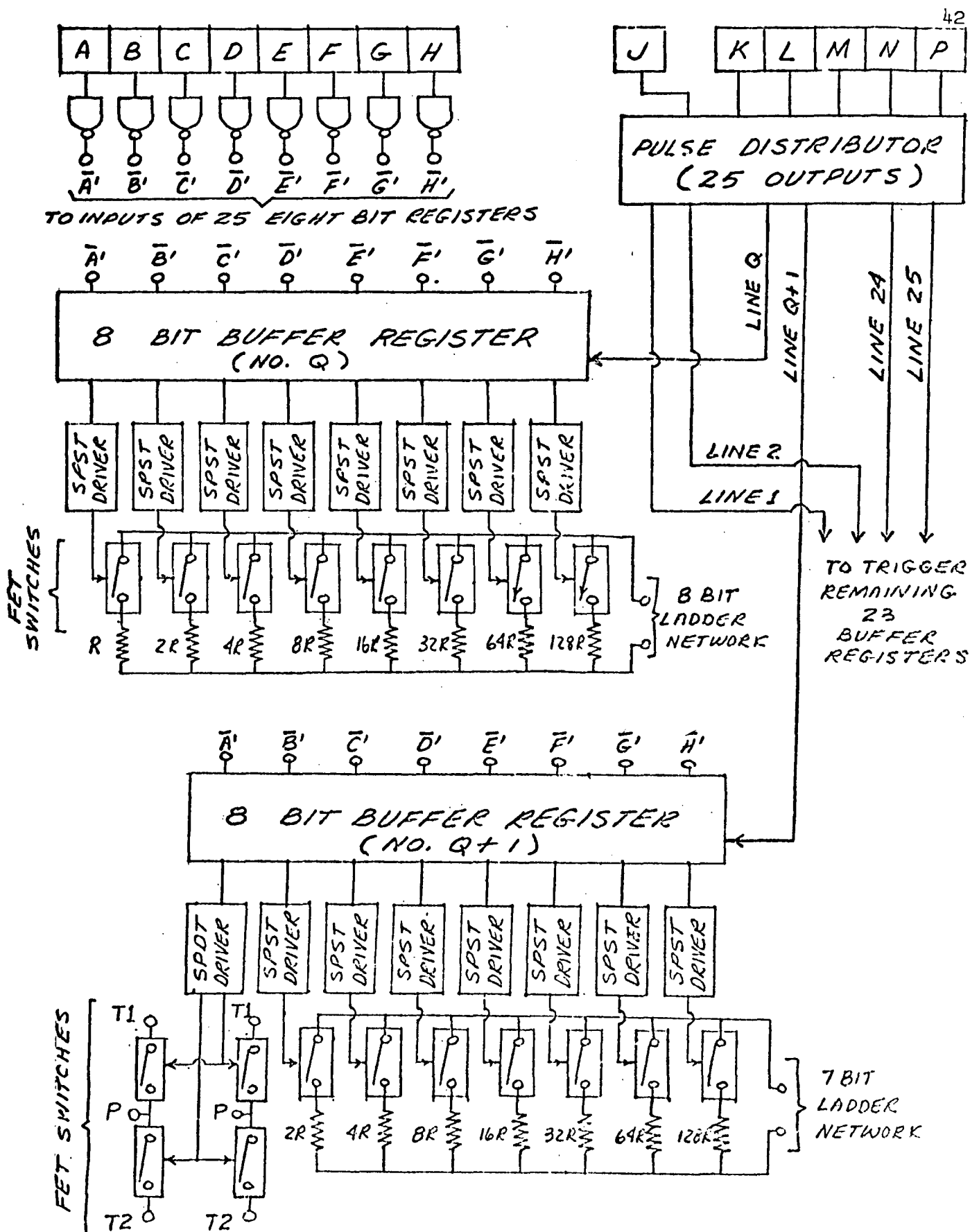
Figure 3-13 The Level Control Stage

Figure 3-14   Digital Computer Control of Conductances
And Analog Switches

store all the information necessary to control the shape of the desired nonlinearity. One Texas Instrument type SN 74199 integrated circuit in a 24 pin dual-in-line package is used for each 8 bit buffer storage register.

An 8 bit word present in output register A-H can be transfered into buffer register Q by applying a trigger pulse through trigger line Q to the trigger input of register Q. Here $1 \leq Q \leq 25$. A trigger pulse occurs on line Q when the content of the address code output register, register K-P, of the Athena is equal to Q, that is, when

$$Q = P + 2N + 4M + 8L + 16K$$

<div align="right">(3.29)</div>

and when the enable bit output register, register J, is equal to 1. Standard transistorized nand gate logic on printed circuit cards is used in the pulse distributor to accomplish this addressed triggering. The pulse distributor contains 25 six input nand gates and eleven inverting pulse amplifiers.

The content of each of the 8 sections of each of the 25 buffer storage registers is connected to the input of either a SPST or a SPDT FET (field effect transistor) driver circuit. The SPST driver contains two bipolar transistors and produces a ± 15 volt output which drives the gate of a symmetrical N channel 2N5459 FET switch. The SPDT driver contains three bipolar transistors and produces a pair of complimentary ± 15 volt outputs which can drive the gates of a pair of 2N5459 switches to form a SPDT switch as required for SW3, or can drive the gates of two pairs of 2N5459 switches to form two synchronous SPDT switches, as required for SW1 and SW2. A SPDT driver controlling a synchronous pair of SPDT switches is diagramed in the

lower left corner of Figure 3-14

Buffer register Q, the 8 SPST drivers, the 8 SPST FET switches, and the 8 ladder resistors make up one digitally controlled 8 bit conductance $G_{\Delta H}$ and are all mounted on a 4 inch by 4 inch printed circuit card. Buffer register Q + 1, its 8 drivers, 11 switches, and seven ladder resistors make up one digitally controlled 7 bit conductance G_{IO} and two SPDT switches SW1 and SW2, and are all mounted on a 4 inch by 4 inch printed circuit card. Conductance $G_{\Delta V}$ and SPDT switch SW3 are mounted on a third 4 inch by 4 inch card.

There are eight sets of five operational amplifiers, one for each segment of the eight segment nonlinear function. Fairchild type μA709 operational amplifiers in 8 pin TO-5 cases are used with each set of five amplifiers mounted on one 4 inch by 4 inch printed circuit card.

11). Software Formats and Generator Load Programs

The coordinates of the nine points (x_I, y_I), $1 \leq I \leq 9$, were read into the memory of the Athena in the form of 18 eight bit words where the most significant bit specified the algegraic sign of x_I or y_I and the remaining seven bits specified the magnitude of x_I or y_I. The most significant of the seven bits represents 5.000 volts, the least significant represents 0.078 volts. There is one minor constraint that the x_I values must satisfy in addition to Inequality 3.1. Since $V_{IO} = (0.5)(x_{I+1} + x_I)$, the binary sum $x_{I+1} + x_I$ must have a zero in its least significant bit if the magnitude of V_{IO} is to be represented by the seven bit code described earlier. This constraint is equivalent

to requiring the x_I and x_{I+1} points to be spaced by some multiple of 0.156 volts.

From the nine stored coordinates the Athena then implemented equations 3.2, 3.3, and 3.4 to compute the three parameters V_{IO}, ΔV_I, and ΔH_I for each section, and loads these parameters into the buffer storage registers (memory) of the DCNFG. The Athena also computes V_{LEVEL} using the fact that V_{LEVEL} is the y_I coordinate of the section having the smallest non-negative V_{IO} value.

C. Applications

1). Sound-Velocity Profile Characterization

The first application of the DCNFG has been in characterization sound-velocity profiles which in turn are related to the problem of acoustic focusing.

The use of the DCNFG in this problem is indicated in Figure 3-15. The same technique, hardware, and programming is used in the profile optimi-zation as in the linear model optimization with the exception of the DCNFG which accepts the parameter p_i from the digital computer output. The given sound velocity data is generated by the digital parameter unit (DPU) previously designed and constructed. The approximating profile is obtained at the output of the DCNFG under control of the parameters p_i which determine the values of sound velocity (y) for specified values of altitude (x). Typical sample results are shown in Figure 3-16 which indicates the performance index, given data, and model profile at the beginning, during optimization, and at termination of the program. Typical run times are 3 to 4 minutes with maximum
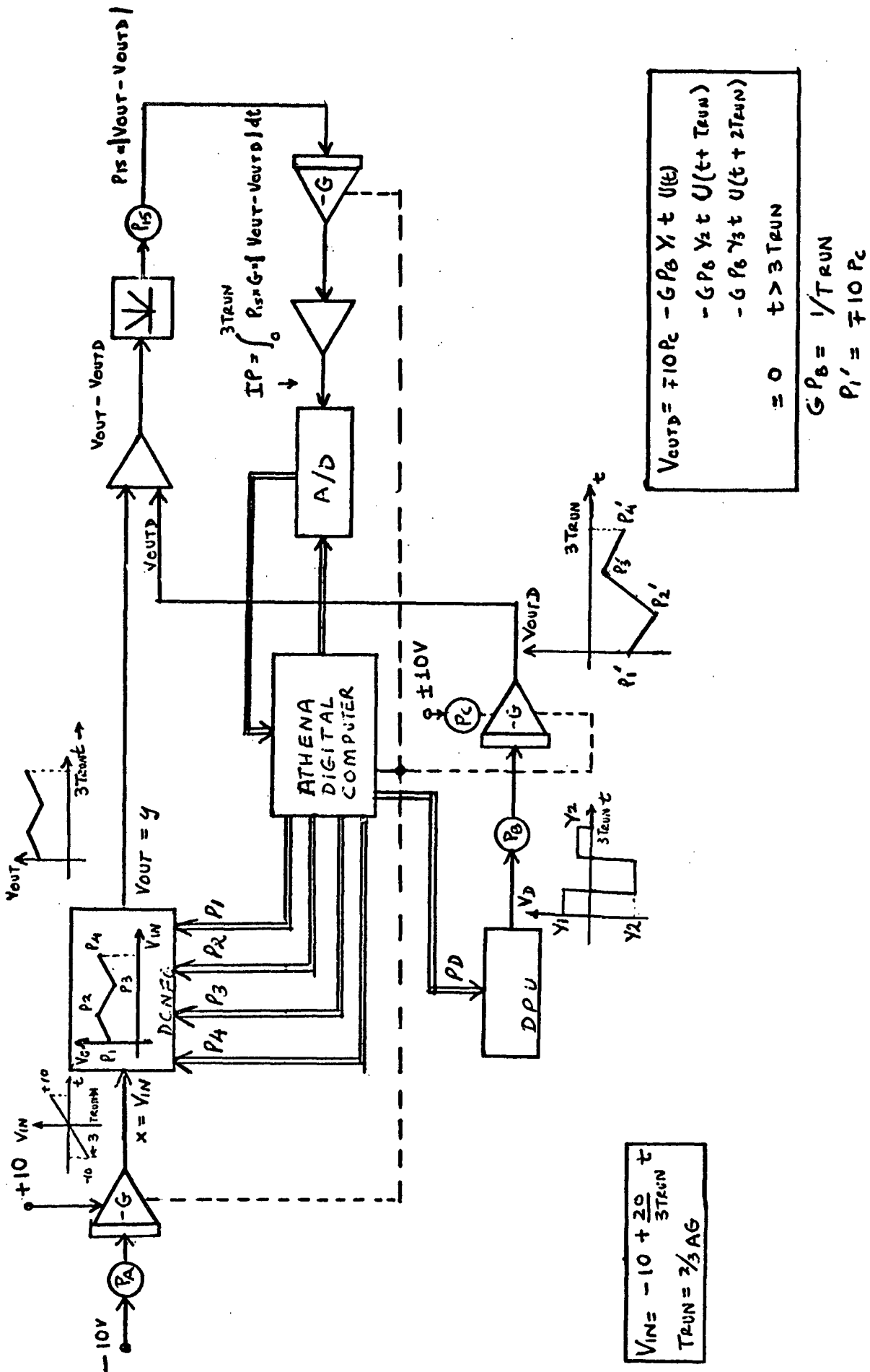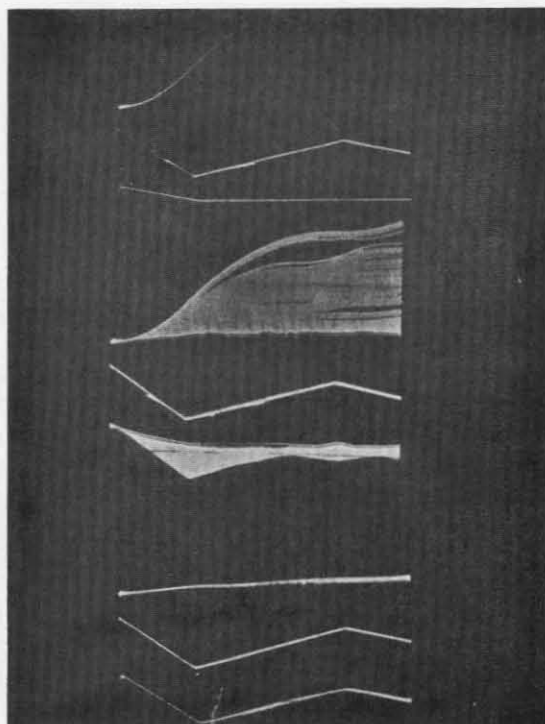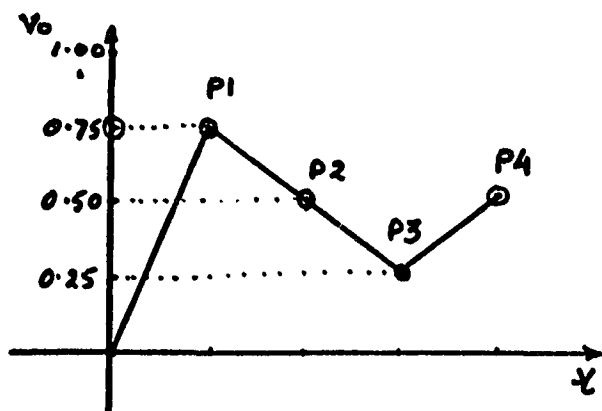
Figure 3-15 Sound Velocity-Profile Characterization

Figure 3-16(a)   Sound-Velocity Profile Characterization

P1 P2 P3 P4 (graph, Vo vs t)

PAR	DEC.	SIGN	BINARY							OCT.
P1	+0·75	1	1	1	0	0	0	0	0	7000
P2	+0·50	1	1	0	0	0	0	0	0	6000
P3	+0·25	1	0	1	0	0	0	0	0	5000
P4	+0·50	1	1	0	0	0	0	0	0	6000

ACTUAL

FUNCTION SET ON THE DPU :

P1 P2 P3 P4 (graph, Vo vs t)
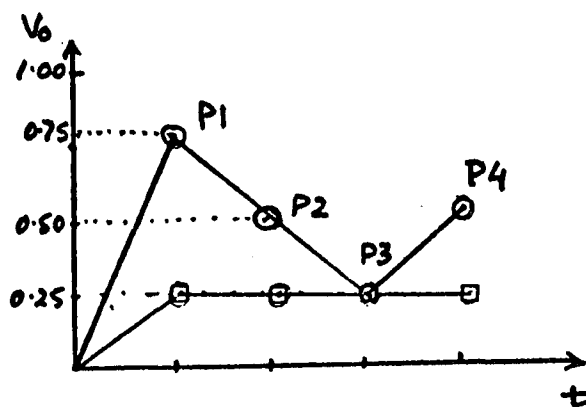
PAR	DEC	SIGN	BINARY							OCT
P1	0·795	1	1	1	0	0	1	0	0	7115
P2	0·518	1	1	0	0	0	0	1	1	6060
P3	0·255	1	0	1	0	0	0	0	0	5040
P4	0·520	1	1	0	0	0	1	0	1	6120

MODEL

FUNCTION ON THE DCNFG: ⊙—⊙ FINAL MATCHED FUNC.
▭—▭ STARTING FUNCTION.

	MODEL.	ACTUAL
P1	0·788	0·750
P2	0·518	0·50
P3	0·255	0·25
P4	0·520	0·50

Figure 3-16(b) Sound Velocity-Profile Characterization

error of 3 to 4 percent at any point on the profile. The parameter set p_i characterizes the profile after the optimization is completed and the program is terminated.

Typical results of the sound velocity profile characterizations are shown in Figures 3-16(a) and (b). In Figure 3-16(a) the oscilloscope display gives the index of performance at the top, the actual sound velocity data in the center, and the estimated profile on the DCNFG at the beginning, during the optimization program, and after the optimization is complete, reading from top to bottom. In Figure 3-16(b) are more detailed results from a typical optimization run which show the given data (set on the DPU) and the initial guess and final estimated profile appearing on the DCNFG.

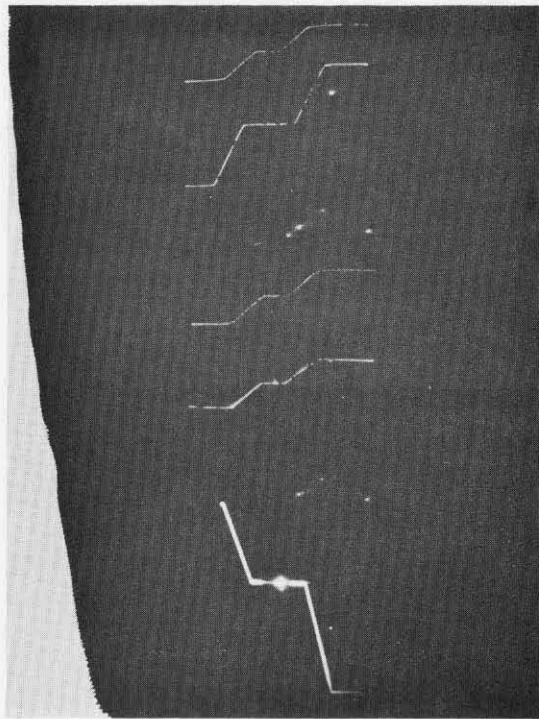## 2). Identification of Nonlinear Dynamic Systems

The identification and design of nonlinear dynamic systems is envisioned as an important area of application of the DCNFG and techniques developed in this work. Feasibility investigations of some simple examples have been completed in the laboratory. In general the actual system was simulated by a nonlinear dynamic system with known nonlinearity and known dynamics. The model to be optimized included the DCNFG and linear dynamics with both linear and nonlinear parameters controlled by the output of the optimization program. The only changes required in the method already described in Part 2 was the addition of the DCNFG to give a computer-controlled nonlinearity.

The results from a typical example are shown in Figure 3-17. The oscilloscope display shows the actual system nonlinearity and the starting guess at the top. The centerpair of figures are the actual system

nonlinearity again and the model nonlinearity after optimization.
The lower figure shows one sign-inverted nonlinearity of the DCNFG
during the optimization run. In addition to the obviously satisfac-
tory identification of the nonlinearity shown here, the linear para-
meter vector identification was also satisfactory.

Good results have been obtained in this problem with both randon and
triangular perturbation signals. However the random signal perturba-
tion is preferred because this is likely to be the nature of the signal
during normal operating conditions, so that no special signal need be
inserted into the actual system. In addition, the need to choose
amplitude and fundamental frequency for a satisfactory triangular
wave can be avioded by use of a random signal with bandwidth covering
the frequency range of interest. The random signal now in use is
gaussian, band-limited white. Other probability densities and fre-
quency characteristics can usually be provided to match specifications
of the signals expected during normal operation. This is accomplished
by certain nonlinear operations on, and filtering of, a gaussian, band-
limited white signal source..

Figure 3-17 Nonlinear Dynamic System Identification
Typical Results

PART 4 EXTENSIONS NOW IN PROGRESS

A. Identification and Design of Multivariable Linear Dynamic Systems

An unforeseen application of the digital controlled nonlinear function generator (DCNFG) has been its use in identification of multivariable linear systems based on experimental test data, or design of such systems to predetermined specifications.

During the work on the DCNFG it was realized that this device provides a possibility of extending the techniques already developed and previously applied to single-input, single-output systems. By storing multiple input-output measurement or specification function pairs and then closing an additional logic loop around the existing program it is anticipated that the matrix transfer function of multivariable linear dynamic systems can be obtained. It is also believed that the speed advantages of the hybrid computing system over the digital computing system will be of the order of n^2 for an nxn matrix transfer function. If this is true, then the class of systems that can be successfully identified, and thereby controlled, in real time by hybrid means but not by all-digital means will have been further widened. It is anticipated that the model so obtained will be in the "P - canonical form" of Mesarovic [8], and will provide a much-needed connection between theory and practical usefulness.

This extension is being pursued by Mr. T. Mather and it is expected to be published for the benefit of the general engineering audience.

B. Topological Aspects of Modeling Nonlinear Dynamic Systems

In preparing for the application of the digital controlled nonlinear function

generator (DCNFG) to the identification and design of nonlinear dynamic systems

certain conceptual progress was required. It has become apparent that the model

topology is important. Both cascade [9] and parallel [6] model topologies have

been suggested and implemented for this class of problems. A basic difficulty

with the cascade, or series, arrangement is that the inverse nonlinear system

must be implemented. This inverse system may not exist at certain points

and may not be single-valued even though the original nonlinear system is

single-valued. As an alternate to the cascade and parallel modeling, an

arrangement using a combination of parallel nonlinearity N_m with cascade linear

inverse and dynamics with realization terms G_{IR} is being investigated as sug-

gested in Figure 4-1. This extension is being investigated by Mr. W. Pool and

will be extracted for publication in an engineering journal.

C.   Development of Models for Human Operator as a System Component

The improvements in techniques and developments in hardware under this

contract have provided the basis for attempting to improve the existing models

of the human operator for use in control system design. This extension is

being pursued by Mr. M. Rouziek.

D.   General Pattern Classification - The Learning Machine Approach

As a result of the successful design of the DCNFG and initial, but incom-

plete, application towards the categorization of sound-velocity profiles, a

rather general problem has come into focus:

Given the set of patterns (sound velocity profiles) and given a binary
function of these patterns (acoustic focusing either occured or it did
not), how can future values of the function (acoustic focusing) best be
predicted from future patterns (sound velocity profiles) that may occur?

This appears to be a very good practical problem by which to test the

progress of Mr. A. Asthana who already has begun investigation into the pattern

recognition problem in connection with learning machines [10]. The results of NASA acoustic focusing measurements or computer programs may be required in order to investigate the learning machine approach.

All of these extensions are being carried out under the director of this project, Dr. Robert L. Drake.
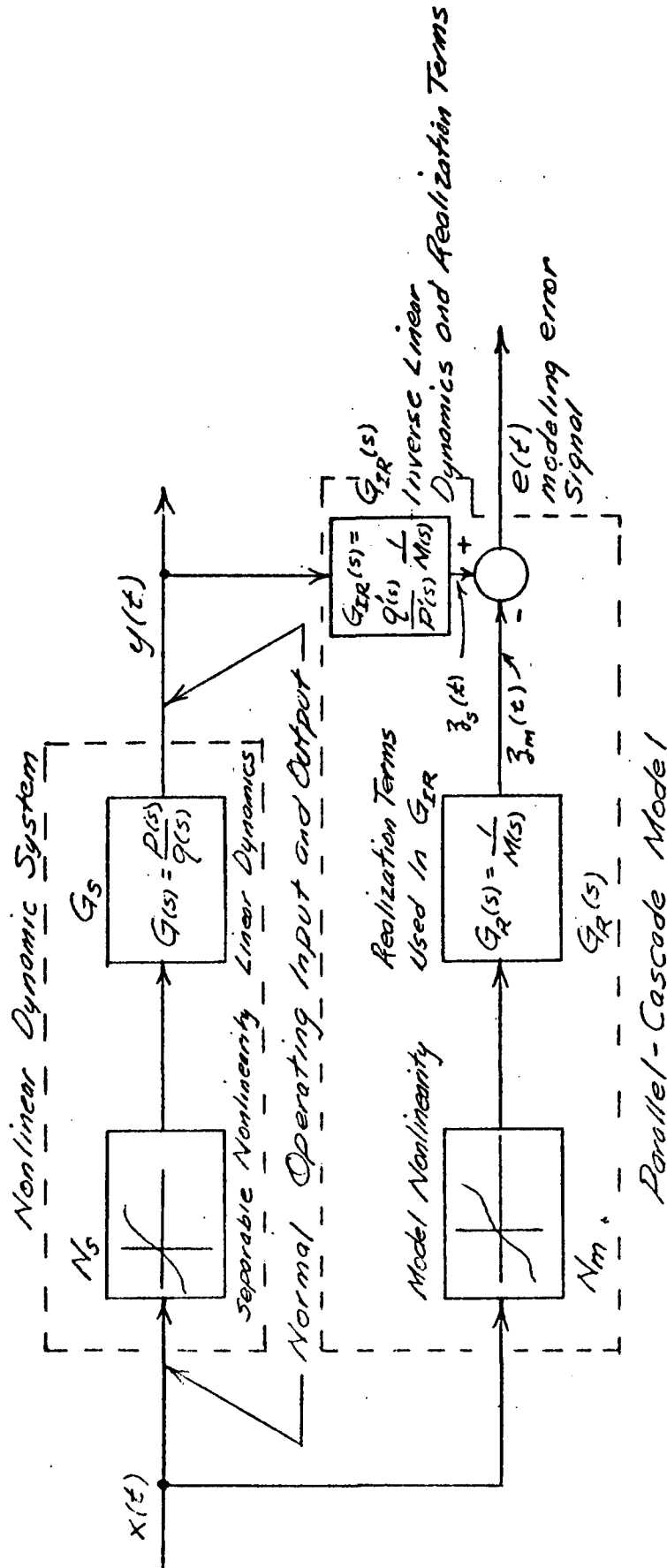
Figure 4-1 Parallel-Cascade Modeling.

PART 5 EFFECT OF THIS RESEARCH UPON ACADEMIC PROGRAMS

In this work the academic disciplines of control, computers, optimization, and signal processing have been applied to the research problem. On the other hand, the research work performed under this contract has affected the nature and character of certain courses by providing concrete problems, physical motivation, and appreciation by the students of the rigors of practicality.

Specific effects of this research upon the academic program that can be cited are:

1). Certain problems have been suggested for use in EE/CHE 743 Adaptive Control and Optimization (Fall 1971) along with the motivation for inclusion of learning system topics in this course for the first time.

2). Several topics have been suggested for inclusion in EE/CHE 744 Control Systems Seminar (Spring 1972), including detailed investigation of certain pattern recognition ideas and learning machines.

PART 6 CONCLUSIONS

A. The principal new results under this contract are the following:

1). The concept of failure mode prediction has been implemented, tested and verified in the laboratory. The advantages of parameter signature analysis over signal signature analysis in determining present readiness of an existing system also have been demonstrated. Typical laboratory results are indicated in Figures 2-6 and 2-7 and are discussed in Part 2 of the report. These concepts are now believed ready for application under the rigors of practicality.

2). The optimization programs in use have been significantly improved by including the Fletcher-Reeves algorithm, successive line searches, and steepest descent starts in the hybrid computer mode of operation. The speed advantage of hybrid computation over all-digital computation ranges from 10/1 to 1000/1 depending upon system order of the dynamic system. Operational cost advantages of hybrid computation are about 5/1 and initial investment cost advantages of hybrid computation are about 10/1.

3). The improved modeling techniques have been applied to a physical example (not a simulation). Excellent results in the identification of the position servomechanism, with no apparent noise problems, have been obtained as indicated in Part 2 (B)(3).

B. A greatly improved digital controlled nonlinear function generator (DCNFG) with practical capability has been designed, implemented, de-bugged, and applied. This device has been completely documented for the use of others. The cost advantage over now-available commercial models may be significant.

C. The DCNFG has been applied to characterizing sound-volocity profiles. This provides an initial step in categorizing such profiles and relating the categories to the problem of acoustic focusing. Some conceptual progress has been made on the categorization problem, but application may be dependent upon the availability of acoustic focusing measurements, computations, or other experience required to teach a learning machine.

D. Several extensions of this work are now in progress by the project director and graduate students as listed in Part 4. Selected ones of the extensions can be accelerated and refined to meet practical requirements, dependent upon the availability of future funding.

E. One publication [11] based on a part of the work reported here has already resulted. At least two other publications are anticipated in the future, as mentioned in Part 4.

PART 7 REFERENCES

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9. R. A. Mathias, "Multivariable Controller Design by Signal Flow Graph Techniques", IEEE Trans. Automatic Control, volume AC-8, number 4, October, 1963, pp. 283-292.

10. N.J. Nilsson, Learning Machines (book), McGraw-Hill, New York, 1965.

11. R. L. Drake, A. Asthana, and T.W. Mather, "Practical Problems and Solutions In Modeling Physical Systems With Time-Domain Input-Output Measurements Or Specifications", Proc. IEEE Region 3 Conference, University of Tennessee, April 10-12, 1972.

PART 8 ACKNOWLEDGMENT

PART 9 APPENDICES
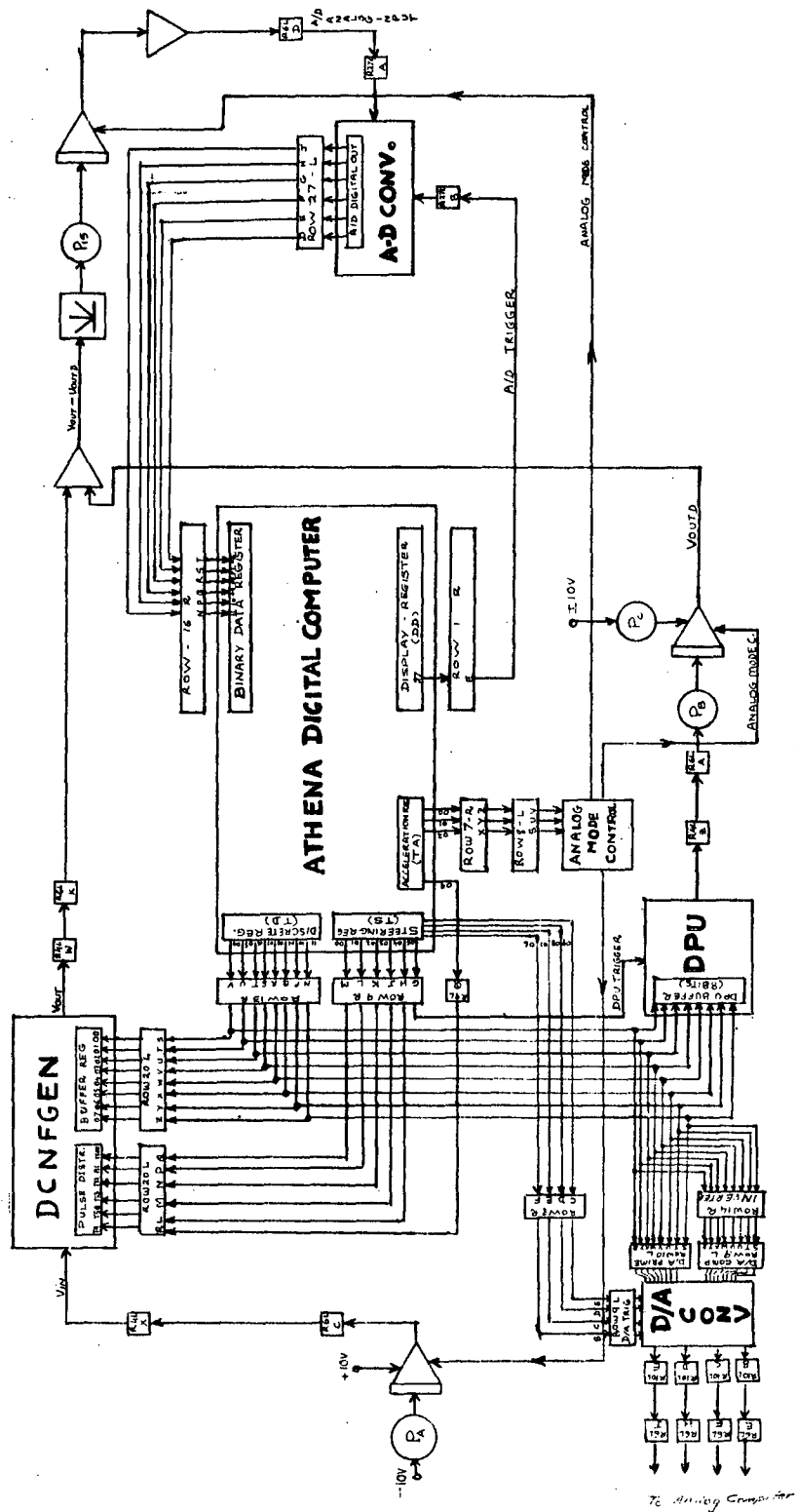
Figure A-1 System Diagram
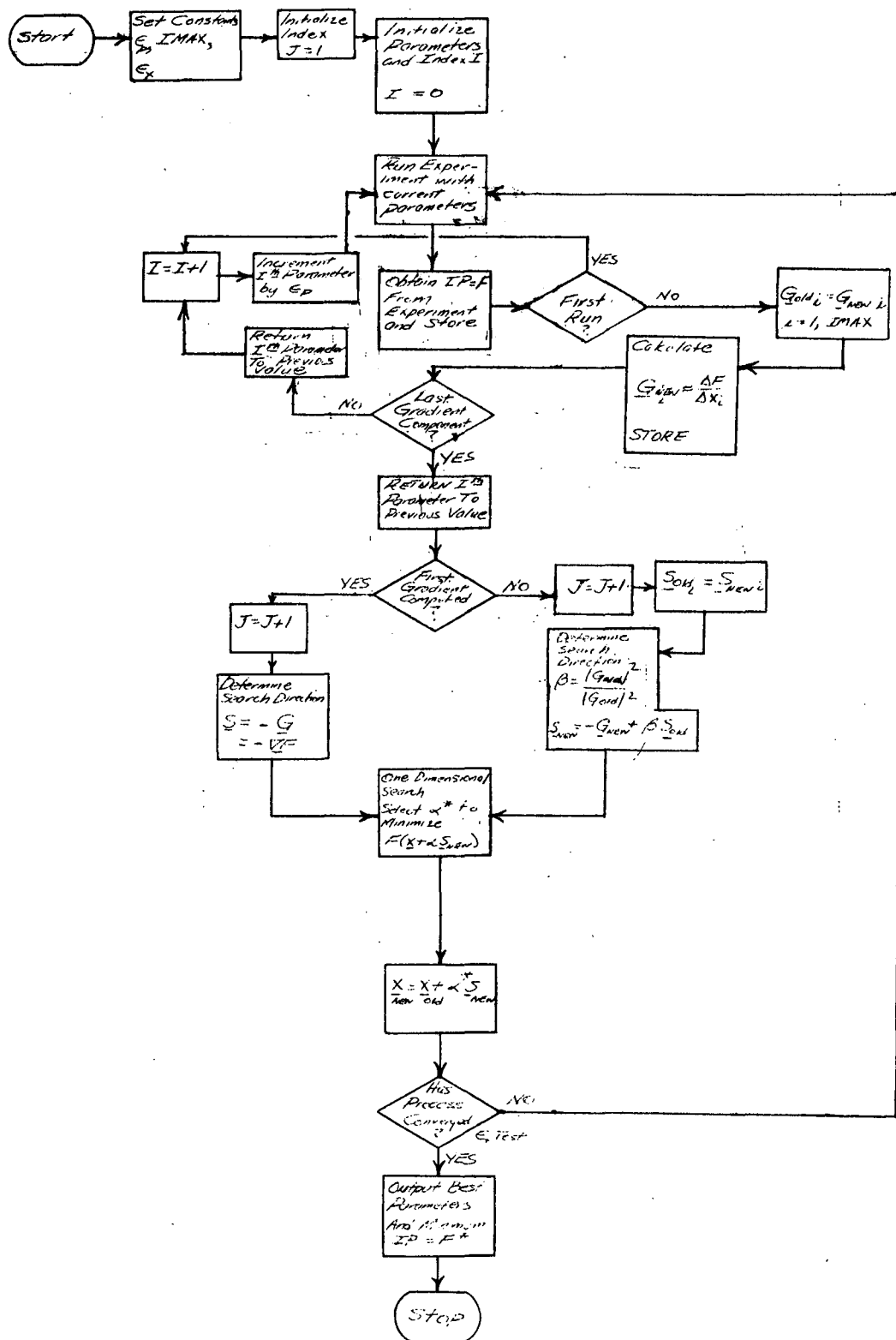
Figure A-2 Optimization Program

Figure A-3 One-Dimensional Search
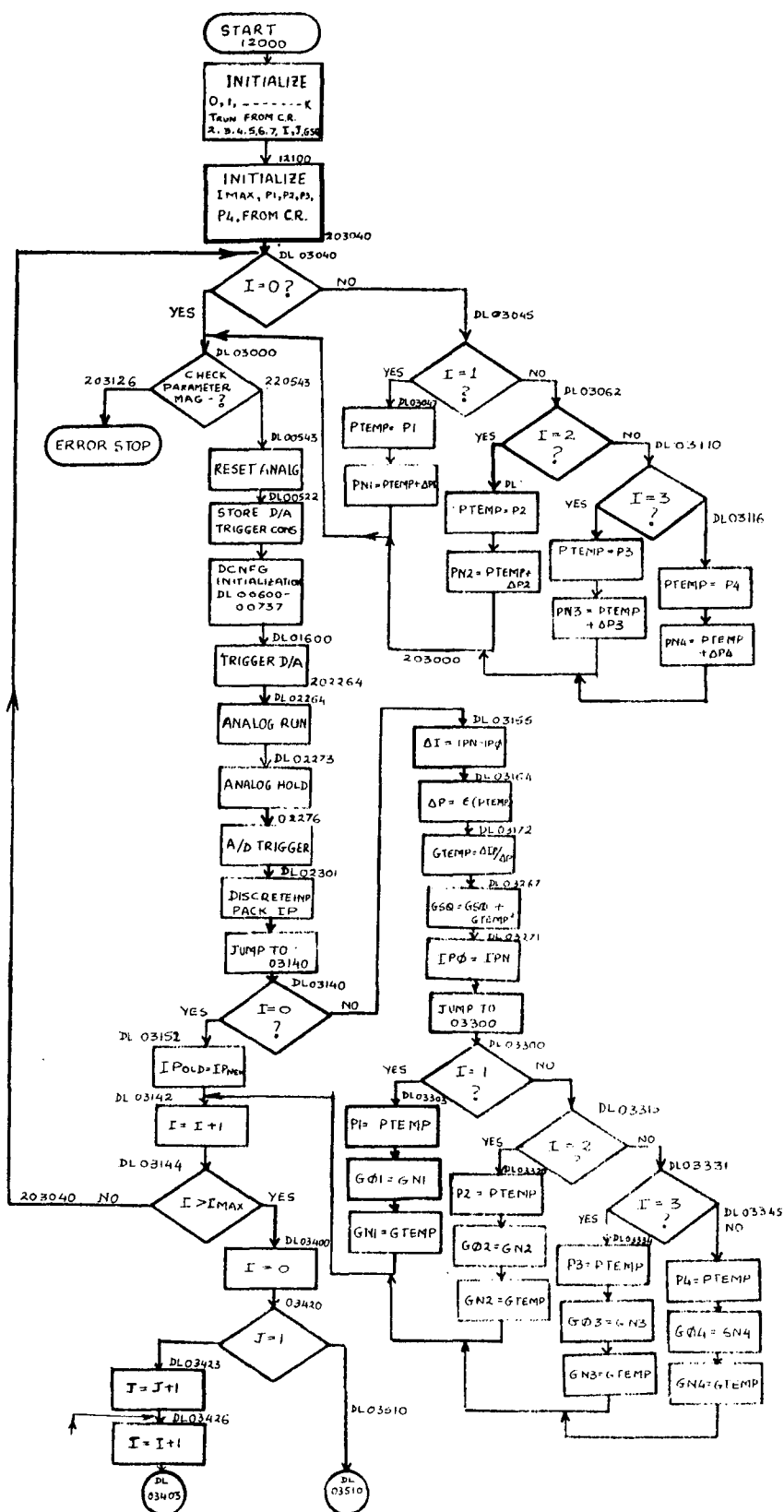
Figure A-4 Gradient Calculation (Sheet 1 of 2)

Figure A-4 Gradient Calculation (Sheet 2 of 2)

ENTER

INITIALIZE AHIGH, ALOW, λ, TAUSQ, KSS, K — DL 06100

$K = K + 1$ — DL 06123

$P1_\lambda = P1 + \lambda \times S1$ — DL 06132

$P2_\lambda = P2 + \lambda \times S2$ — DL 06140

$P3_\lambda = P3 + \lambda \times S3$ — DL 06146

$P4_\lambda = P4 + \lambda \times S4$ — DL 06154

STORE K_A — DL 06264

STORE DEC. CONST. — DL 06512

COPY DEC. CONST. — DL 07322

DEC. CONST. = 0 ?

STORE PAR. IN GRAD CL. — DL 07326

GRAD PROG.

YES — D/A TRIGGER ANALOG RESET — DL 06267

CHECK PAR. MAG. — DL 06473

NO — ERROR STOP — DL 07100

YES — ANALOG RUN — DL 07440

ANALOG RUN DELAY — DL 06374

A/D TRIGGER — DL 06312

(A)

$P1_{\lambda_P} = P1 + \lambda_P \times S1$ — DL 06203

$P2_{\lambda_P} = P2 + \lambda \times S2$ — DL 06211

$P3_{\lambda_P} = P3 + \lambda \times S3$ — DL 06271

$P4_{\lambda_P} = P4 + \lambda \times S4$ — DL 06225

(B)

$P1_{\lambda_N} = P1 + \lambda \times S1$ — DL 06231

$P2_{\lambda_N} = P2 + \lambda \times S2$ — DL 06244

$P3_{\lambda_N} = P3 + \lambda_N \times S3$ — DL 06252

$P4_{\lambda_N} = P4 + \lambda_N \times S4$ — DL 06260

(C)

$\lambda_P = \lambda + E_\lambda (AHIGH - ALOW)$ — DL 06166

$\lambda_N = \lambda + E_\lambda (AHIGH - ALOW)$

(A)

$K_A = K_A + 1$

$K_A - 1 = 0$ — NO / YES

$K - 2 = 0$?

ENTER PIN — DL 06336

ENTER P1P — DL 06331

ENTER P1∅ — DL 06315

D

B

C

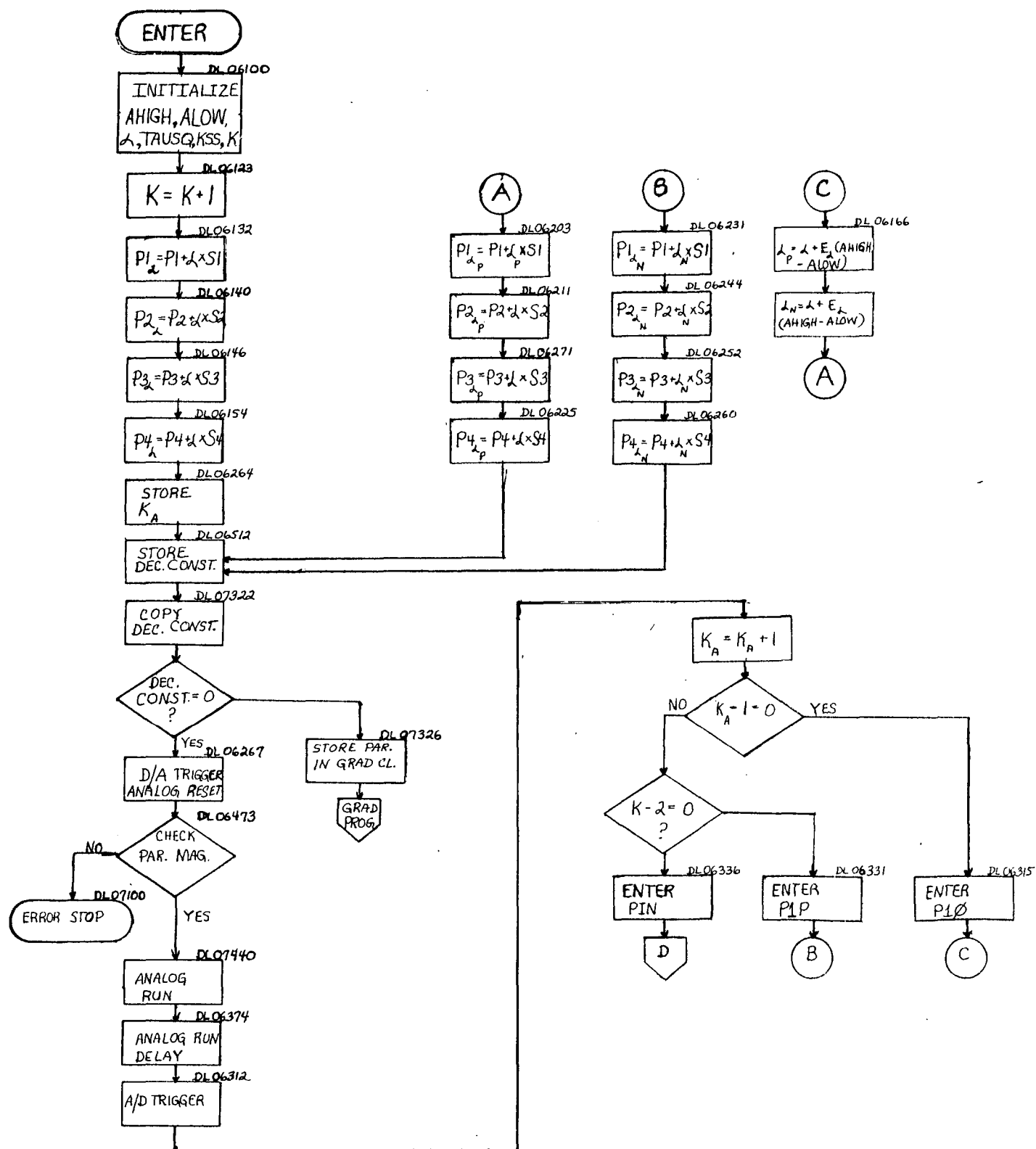Figure A-5 One-Dimensional Search (Sheet 1 of 3)
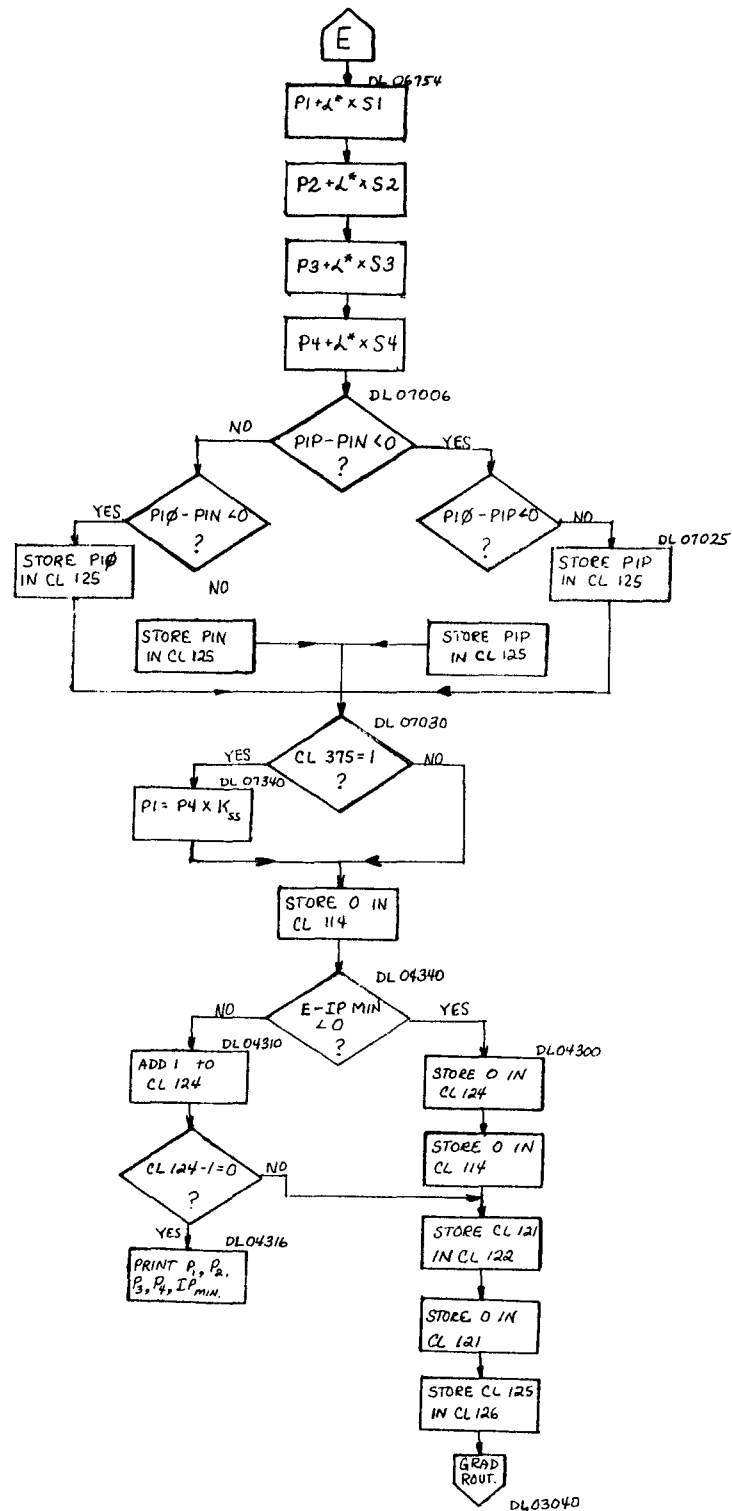
Figure A-5 One-Dimensional Search (Sheet 2 of 3)
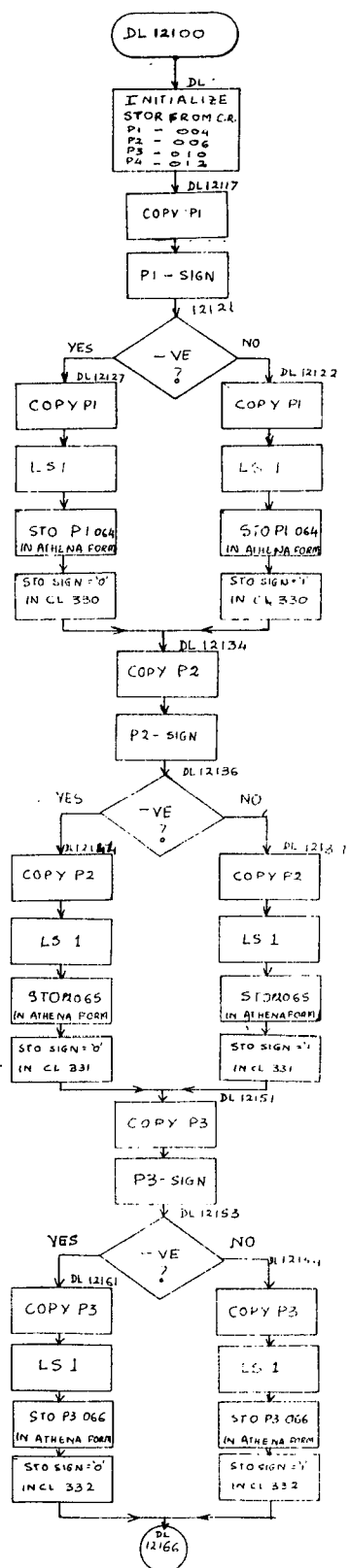
Figure A-5 One-Dimensional Search (Sheet 3 of 3)

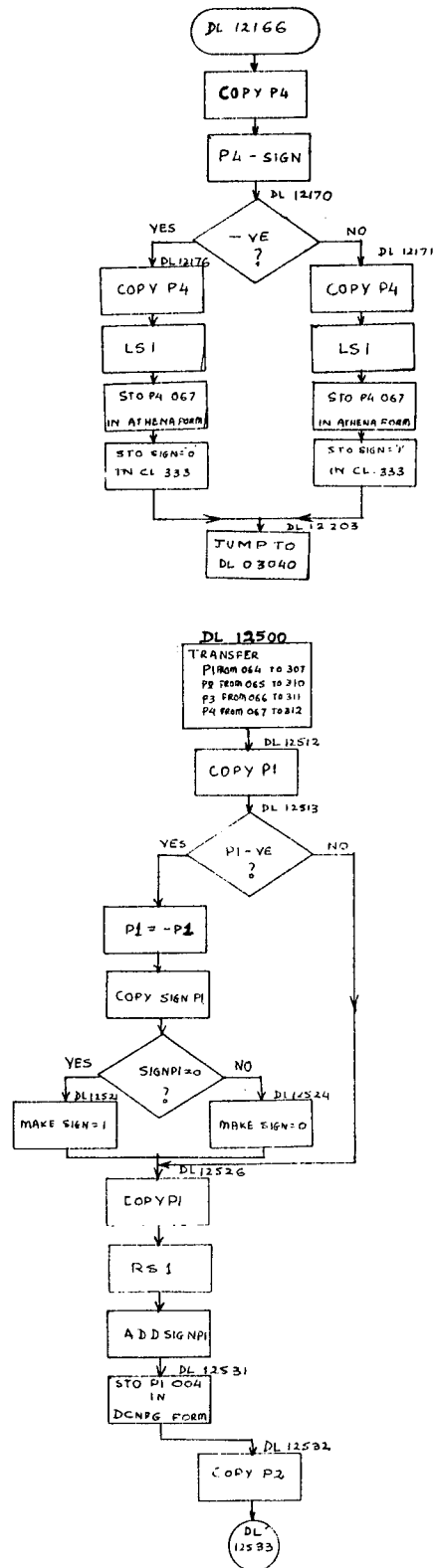Figure A-6 Control Program for DCNFG (Sheet 1 of 4)

Figure A-6 Control Program for DCNFG (Sheet 2 of 4)

DL 12533

P2 -VE ?　YES　→　DL12535　No　12546

P2 = -P2

DL 12537
COPY SIGN P2

DL 12540
SIGN P2 = 0 ?　YES　→　DL 1254
NO　→　DL 12544

MAKE SIGN P2 = 1

MAKE SIGN P2 = 0

DL 12546
COPY P2

RS 1

ADD SIGN P2

DL 12551
STO P2 006 IN DCNFG FORM

DL 12552
COPY P3

DL 12553
P3 -VE ?　YES　→　DL 12555　NO　→　DL 12566

P3 = -P3

DL 12557
COPY SIGN P3

DL 12560
SIGN P3 = 0　YES　→　DL 12561　NO　→　DL 12564

MAKE SIGN P3 = 1

MAKE SIGN P3 = 0

DL 12566
COPY P3

RS 1

ADD SIGN P3

DL 12571
STO P3 010 IN DCNFG FORM

DL 12572
COPY P4

12573
P4 -VE ?　YES　→　12575　NO　→　DL 12606

P4 = -P4
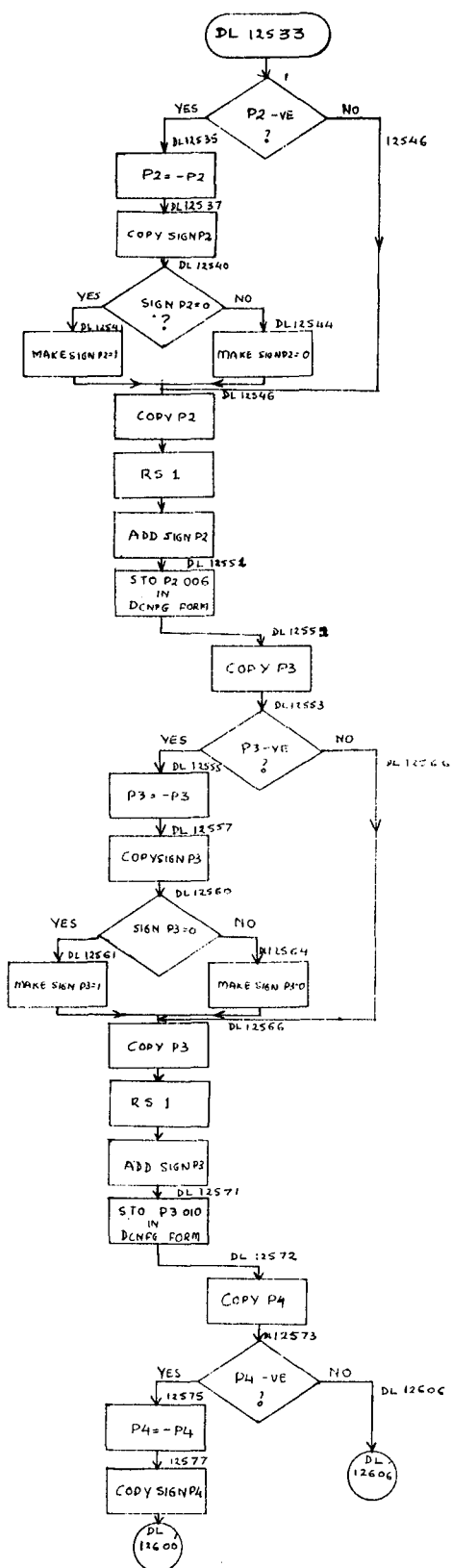
12577
COPY SIGN P4

DL 12600

DL 12606

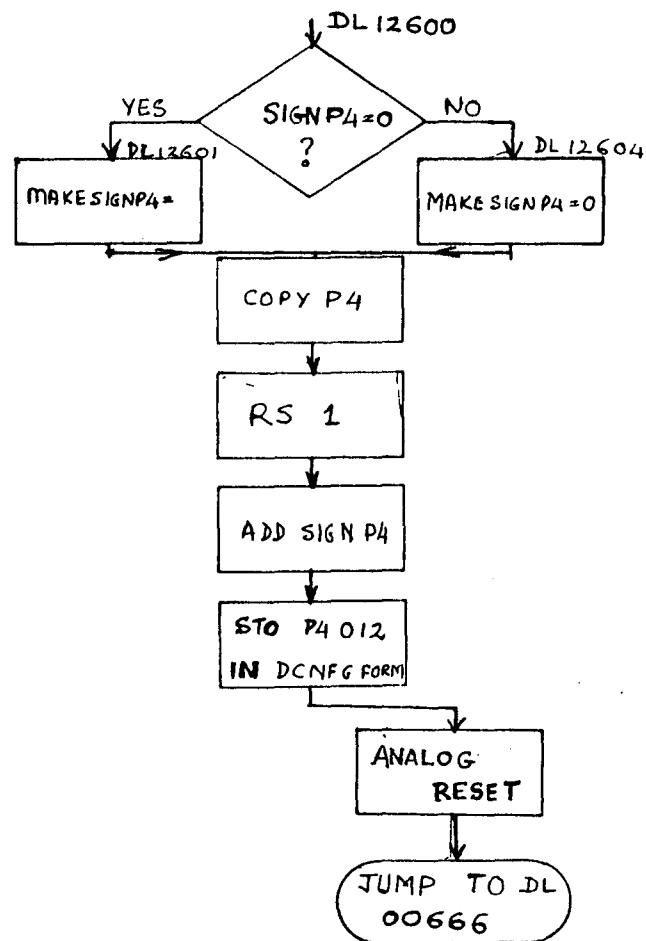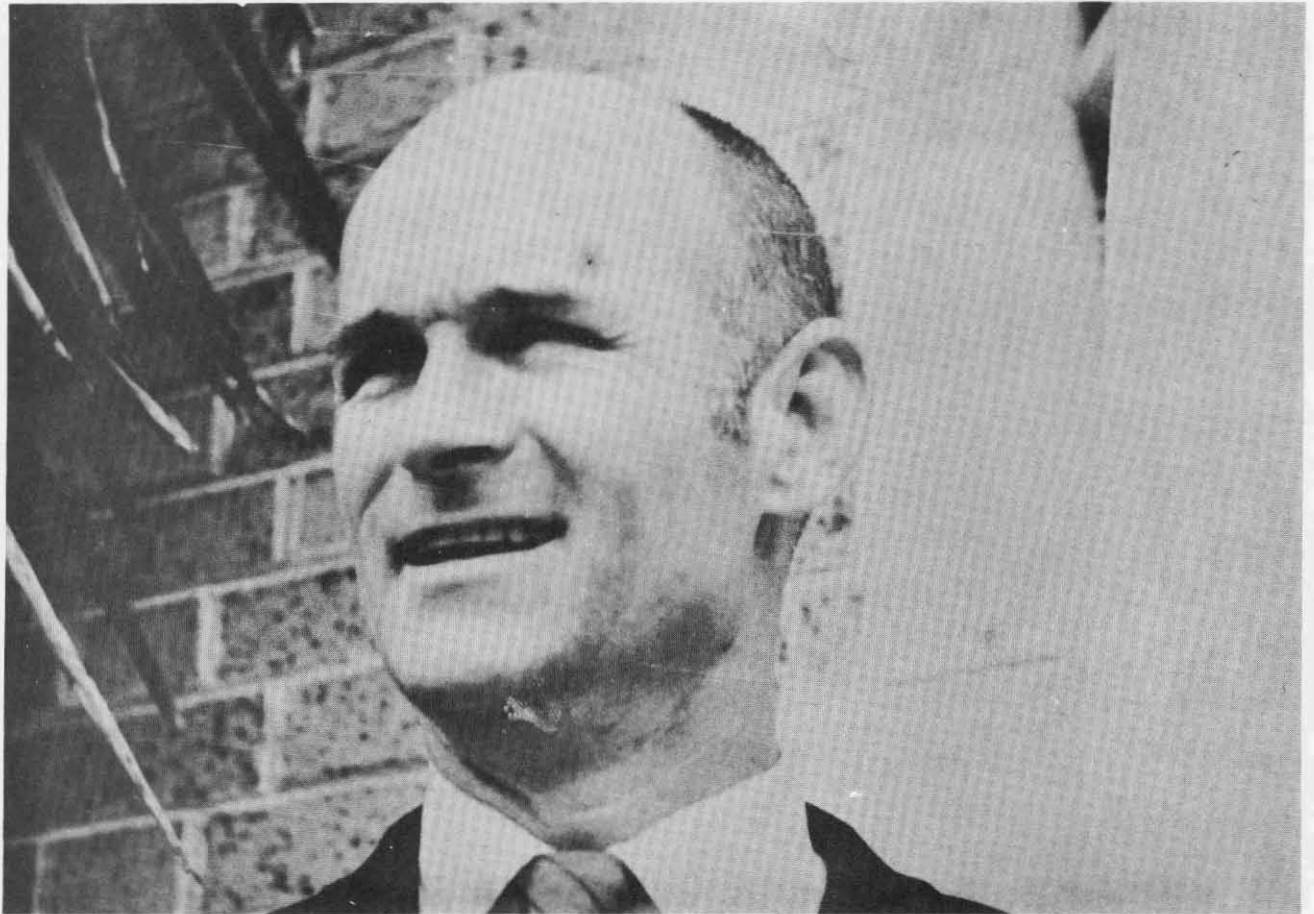Figure A-6 Control Program For DCNFG (Sheet 3 of 4)

Figure A-6 Control Program For DCNFG (Sheet 4 of 4)

Dr. R.L. Drake
Project Director

Contributions to concepts of digital controlled nonlinear function
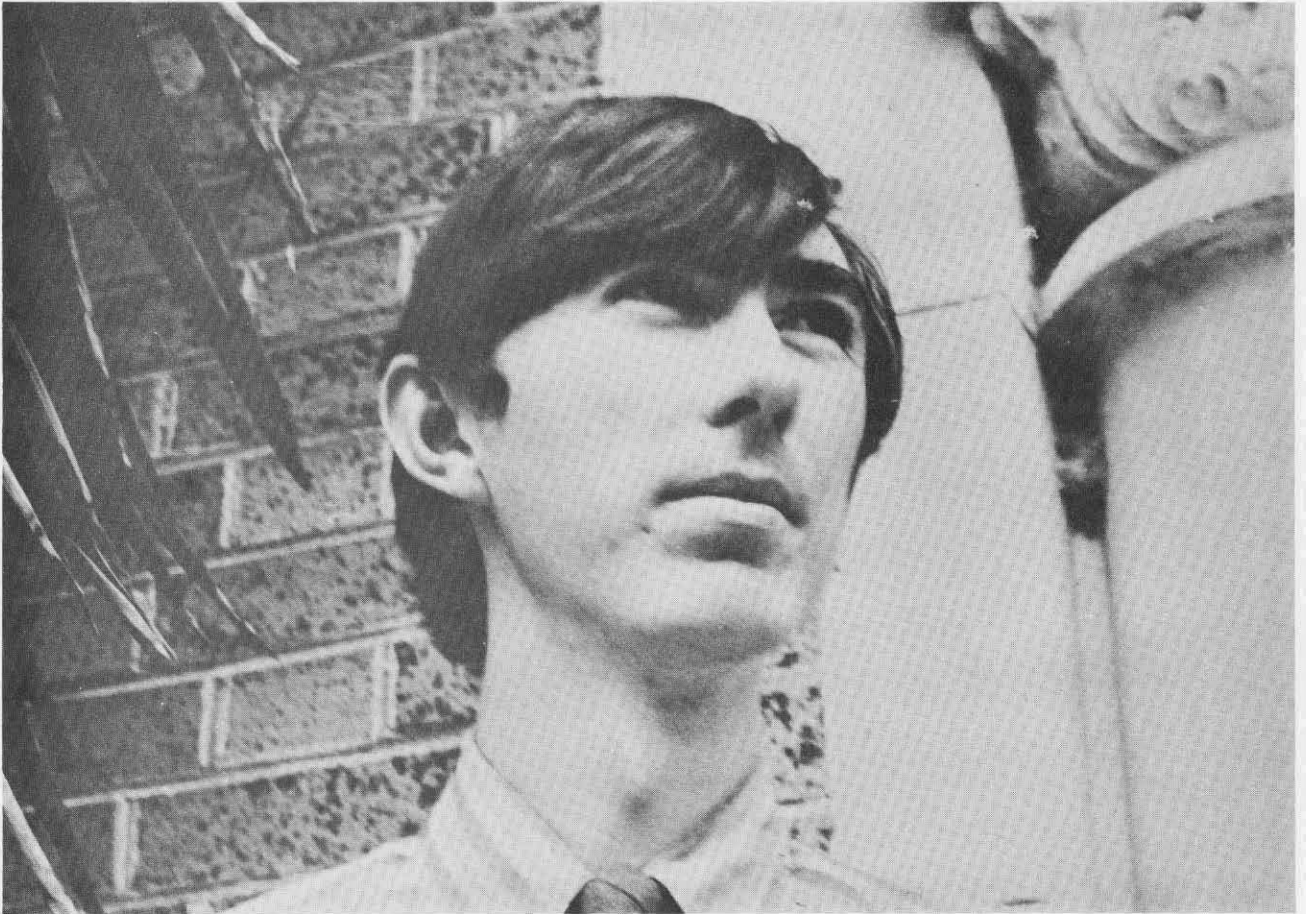generator, software, and problem solutions.

Dr. P.F. Duvoisin

Investigator

Contributions to concept, design, and implementation of digital
controlled nonlinear function generator.

Mr. A. Asthana

Research Assistant

Contributions to all phases of hardware, software, and problem solutions.

Mr. T. Mather

Research Assistant

Contributions to software and problem solutions.